System Controller

Small scale SMP system 1~4 CPU’s

CPU

System Controller (North Bridge)

RAM

High Bandwidth I/O

Low Bandwidth I/O

I/O Controller (Southbridge)
Play Games?

Heavy demand placed on memory system
Heavier still in SMP/SMT/CMP system
System Controller == System traffic cop
**System Controller: Athlon**

- **CPU**
- **BIU1**
- **BIU0**
- **AGP**
- **APC**
- **MRO**
- **MCT**
- **PCI**
- **DRAM**

**Abbreviations:**

- **MRO**: Memory Request Organizer
- **APC**: AGP PCI Controller block
- **MCT**: Memory Controller (SDRAM/DDR/DRDRAM)
**MRO**: Memory Request Organizer

- Request crossbar responsible for scheduling memory read and write requests from BIU, PCI, AGP
- Serves as the coherence point
- Requests are reordered to minimize page conflict and maximize page hits
- Anti-starvation mechanism by aging of entries
- Arbitration bypassed during idle conditions to improve latency
## AMD Athlon Controller:

### Silicon Stat

<table>
<thead>
<tr>
<th>Chip Version</th>
<th>Tech &amp; Voltage</th>
<th>Max Core Speed</th>
<th>Die Size (pad limited)</th>
<th>No. of pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDRAM 1P, 2xAGP</td>
<td>0.35um, 3.3V</td>
<td>100 MHz</td>
<td>107 mm²</td>
<td>492</td>
</tr>
<tr>
<td>SDRAM, 2P, 2xAGP</td>
<td>0.35um, 3.3V</td>
<td>100 MHz</td>
<td>130 mm²</td>
<td>656</td>
</tr>
<tr>
<td>DDR, 1P, 4xAGP</td>
<td>0.25um, 2.5V</td>
<td>133 MHz</td>
<td>133 mm²</td>
<td>553</td>
</tr>
<tr>
<td>DDR, 2P, 4xAGP</td>
<td>0.25um, 2.5V</td>
<td>133 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RDRAM, 1P, 4xAGP</td>
<td>0.25um, 2.5V</td>
<td>133 MHz</td>
<td>107 mm²</td>
<td>492</td>
</tr>
</tbody>
</table>
AMD Athlon Controller:

Die photo: SDRAM, 2P, 2xAGP

Approx. 500K gates
11.43x11.43mm²
Cache Coherency I

Read Request: I would like data for cacheline 0x001CA980
Cache Coherency II

Snoop Request: Do you have cacheline 0x001CA980?
Memory Fetch: Give me data for 0x001CA980.
Cache Coherency Illa

Snoop Response: No
SDRAM MCT: RAS to rank 2, bank 0, row 0x00842
SDRAM MCT: CAS to rank 2, bank 0, col 0x0C3
SDRAM MCT: Here’s the data.
Cache Coherency IIIb

Snoop Response: Yes, I have this cache line
SDRAM MCT: RAS to rank 2, bank 0, row 0x00842
SDRAM MCT: CAS to rank 2, bank 0, col 0x0C3
MRO: Here’s the data.
Why worry about CC?

What if distance to DRAM is shorter than distance to cache (in another CPU)?
Most clock domains are integer multiples of each other.
Multiple Clock Domains II

What if clock domains are not integer multiples of each other?
Multiple Clock Domains III

- FastClk (100MHz)
- SlowClk (66MHz)
- Data
- LatchEn
- Latched Data
- CtlMask

Diagram:
- Slow clock domain
- Fast clock domain
- Gear Box Module

- AMD Athlon Chipset Gearbox Logic

- Dff
- Cmb Logic
- LatchEn
- FastClk
- CtlMask
Multiple Clock Domains IV

Data transfer from 100 MHz clock domain to 133 MHz clock domain (Latency Optimal)

Data transfer from 100 MHz clock domain to 133 MHz clock domain (Bandwidth Optimal)
Multiple Clock Domains V

Data transfer from 400 MHz clock domain to 800 MHz clock domain (Latency Optimal)

Data transfer from 400 MHz clock domain to 800 MHz clock domain (Bandwidth Optimal)
Multiple Clock Domains VI

- CPU Clock Domain (10:2) 500 MHz (harmonic)
- CPU Clock Domain (11:2) 550 MHz (not-harm)
- CPU Clock Domain (12:2) 600 MHz (harmonic)

Processor to Processor Bus Interface

Fractional Multipliers could impact performance, but you may not have a choice.
Multiple Clock Domains VII

AMD Athlon SPEC CPU FP Completion Time

- 1466 MHz
- 1533 MHz
- 1666 MHz
- 1733 MHz
- 1600 MHz

Total Task Time (seconds) vs. Cycle Time (ns)

- Non-Harmonic Node
- Harmonic Node
GART: Graphics Address Remapping Table

“TLB” translation for memory allocated to graphics
Quick Summary I

Transaction Queue (R/W)

Address Mapping

Command Generation

Deep Queue (8~32)
Coherency Check

GART etc. Depending on what user installed

bank open? row match?
CAS only or RAS + CAS?

Timing dependent Control

RAS = 3 cycles
CAS = 2 cycles

Data
Quick Summary II

- System Controller is a “traffic cop”
- Traffic cop may have to deal with clock domain synchronization issue
- Handles Cache Coherency for small scale SMP configuration
- Memory Controller must know everything there is to know about DRAM system. Which bank is in what state, and the appropriate timed command sequence to get data.