Wires Part II and Signalling

- More on transmission lines
- Termination
- Crosstalk
Voltage and Current Mode I

- BJT: Current controlled current source
- MOSFET: Voltage controlled current source
- Current and voltages at output controlled by careful design of resistors values
- “On resistance” of MOSFET is low. “Off resistance” of MOSFET is high
- “resistance” through BJT is always high
Voltage and Current Mode II

- “1” and “0” represented by +/- of voltage or current from transmitter perspective.
- Receiver sees voltage differential.
- No “pure” voltage-mode or current mode.
- $Z_{GT}$ is high. Isolates circuit from noise on power planes.
- If $Z_{out} >> Z_0$, current mode. $Z_{out} << Z_0$, voltage mode.

$V_T = I_T Z_0$
“Wired Or” Bus

- Terminating resistor supplies “1”, voltage on bus is equal to $V_{ddq}$ when no driver is active
- Driver sinks current to $V_{ssq}$ when it needs to drive “0”
- Power consumed when “driving 0” and active current sinks
Capacitive Termination I

- Capacitors behave like short circuit when not charged. Once charged, behaves like open circuit.
Capacitive Termination II

- When “shorted”, $V_S$ is reflected with the same magnitude back toward source.
- The “magnitude” here is the “magnitude” of rise time.
- To minimize glitch, limit slew rate.
What is a Stub?

- Signal path inside of package also significant
Series Stub Terminated Logic

Reflection Coefficient = \( \rho = \frac{Z_L - Z_S}{Z_L + Z_S} \)

\( \rho = \frac{25 - 50}{25 + 50} = -0.3333 \)

- Series resistor isolates stub from line
- reduces ringing
- reduces power
Rambus Signalling

- Current mode
- Controller sends full height signal swings
- DRAM chips send half height signal swings
- Reflection off of controller driver creates full height signal swing
- Current control and voltage slewrate control
ODT: On Die Termination

- Active, dynamic termination, depending on R/W, and number of loads on electrical bus
- Can be turned on/off in 2 cycles, off in 2.5 cycles
- Designed into DDR II
Input Buffering - References I

- **LV TTL Inverter**
  - Input voltage: $V_{in\ low} = 0.8\ V$, $V_{in\ high} = 2.0\ V$
  - Output voltage: $V_{out\ high} = 2.4\ V$, $V_{out\ low} = 0.4\ V$

- **SSTL-2 Inverter**
  - Input voltage: $V_{in\ low} = (V_{ref} - 0.15\ V)$, $V_{in\ High} = (V_{ref} + 0.15\ V)$
  - Output voltage: $V_{out\ low\ full\ current\ drive} = V_{ddq} - 0.373\ V$

**Simple Inverter**

- Input voltage: $V_{ref}$
- Output voltage: $V_{out\ low\ full\ current\ drive} = 0.373\ V$
- Inverters aren’t very good for high frequency signalling
- Local or remote reference?
Differential Signalling

- Send the signal and its complement
- The complement signal path is the current return path
- Signal pairs must be routed closely together
- Signalling scheme can reject common mode noise quite well
Crosstalk I

- Signals should couple to ground to minimize EM.
- If EM fields do not cancel, could induce voltage/current excitation in nearby victim line.
- Magnitude of crosstalk depends on current magnitude current loop area(s) AND signal patterns on “aggressor” lines.
Crosstalk II

- Routing of wires done for path length matching may in fact have slightly different “electrical distance” due to segments of the wire coupling to itself