SDRAM Memory System

“Mesh Topology”


### SDRAM Chip Basics

66, 100, 133 MHz

**Multiplexed Address Bus**

**Programmable Burst Length, 1,2,4,8 or page**

**Quad Banks Internally**

**Supply Voltage of 3.3V**

**Low Latency, CAS = 2 , 3**

**LVTTL Signaling (0.8V to 2.0V)**

(0 to 3.3V rail to rail.)

<table>
<thead>
<tr>
<th>Condition Specification</th>
<th>Cur.</th>
<th>Pwr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating (Active) Burst = Continuous</td>
<td>300mA</td>
<td>1W</td>
</tr>
<tr>
<td>Operating (Active) Burst = 2</td>
<td>170mA</td>
<td>560mW</td>
</tr>
<tr>
<td>Standby (Active) All banks active</td>
<td>60mA</td>
<td>200mW</td>
</tr>
<tr>
<td>Standby (powerdown) All banks inactive</td>
<td>2mA</td>
<td>6.6mW</td>
</tr>
</tbody>
</table>
SDRAM Chip Architecture

256 Mbit chip: 8192 rows, 512 columns, x16 data, 4 banks
Mode Register

Burst Length = 1, 2, 4, 8, or Page mode
CAS Latency = 2, 3 (4, 5, etc in special versions)
Burst Type = Sequential or Interleaved

SDRAM Device can be programmed to respond in slightly different manners
## Command Truth Table

<table>
<thead>
<tr>
<th>Command</th>
<th>CS#</th>
<th>RAS#</th>
<th>CAS#</th>
<th>WE#</th>
<th>DQM</th>
<th>addr</th>
<th>DQs</th>
</tr>
</thead>
<tbody>
<tr>
<td>command inhibit (nop)</td>
<td>H</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>no operation (nop)</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>active (activate row - RAS)</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>X</td>
<td>addr</td>
<td>X</td>
</tr>
<tr>
<td>read (start read - CAS)</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L/H</td>
<td>addr</td>
<td>X</td>
</tr>
<tr>
<td>write (start write - CAS W)</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L/H</td>
<td>addr</td>
<td>valid</td>
</tr>
<tr>
<td>burst terminate</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>active</td>
</tr>
<tr>
<td>precharge</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>**</td>
<td>X</td>
</tr>
<tr>
<td>auto refresh</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>load mode register</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>code</td>
<td>X</td>
</tr>
<tr>
<td>write enable/output enable</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>H</td>
<td>-</td>
<td>active</td>
</tr>
<tr>
<td>write disable/output High-Z</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>L</td>
<td>-</td>
<td>hi-Z</td>
</tr>
</tbody>
</table>

** bank address, or all banks with a _10 assertion
System Initialization

1. Apply power to Vdd and VddQ
2a. Wait 100us before issuing command to DRAM chip
2b. Read out SPD
3. Issue at least one NOP
4. Issue precharge-all command
5. Issue two auto-refresh commands
6. Program mode register
**CAS Read/Write Commands**

- **Read Command**
  - **CAS = 2**
  - **DQ (data bus)**
  - **D out**
  - **t_{OH}**

- **Write Command**
  - **D in**
  - **DQ (data bus)**
Piplined CAS Reads

1. Read command and address assertion
2. Data return from rank #0
3. Clock signal
4. Data return from rank #1
5. Data bus utilization
6. CASL 3
7. SDRAM rank #0
8. SDRAM rank #1
9. Memory Controller
10. Data bus
11. Clock signal
12. Data return from rank #0
13. Data return from rank #1
14. Rank #0 hold time
15. Bus idle time
16. Rank #1 setup time
Write after Read

Clock signal

Data bus

Data return from rank # 0

Data written from memory controller

Rank # 0 hold time

Bus idle time

Setup time

Memory Controller

SDRAM rank # 0

SDRAM rank # 1

Data bus utilization

CASL 3

Read command

Write command
Read after Write

![Diagram of DRAM memory system](image)

**Back-to-back accesses to same rank**

**Back-to-back accesses to different ranks**
Multiplexed Address Bus

- Active
- Command bus
- Read
- Row address
- Address bus
- Column address

$t_{RAS} = 3$

- Address bus
- Address register
- Mode register
- Row address mux
- Column address counter/latch
- Bank control logic
Signaling: LVTTL

- No reference voltage
- Rail-to-rail swing of 3.3V

Input voltage

V\text{in} \text{low} = 0.8V \quad V\text{in} \text{high} = 2.0V

Output voltage

V\text{out} \text{low} = 0.4V \quad V\text{out} \text{high} = 2.4V

- LVTTL inverter

- Rail-to-rail swing of 3.3V
DDR SDRAM Memory System

Same Topology as SDRAM

Single Channel DDR SDRAM Controller

Dimm1 Dimm2 Dimm3

Addr & Cmd
Data Bus
DQS (Data Strobe)
Chip (DIMM) Select
DDR SDRAM Chip

- 100, 133, 166, 200 MHz (200, 266.. etc Mbps)
- Multiplexed Address Bus
- Programmable Burst Lengths, 2, 4 or 8*
- Quad Banks Internally
- Supply Voltage of 2.5V*
- Low Latency, CAS = 2, 2.5, 3*
- SSTL-2 Signaling (Vref +/- 0.15V)
  (0 to 2.5V rail to rail)

Diagram:
- Clk #
- Clk
- Cmd (Read)
- DQS
- Data
- CASL = 2
- DQS Post-amble
- DQS Pre-amble

256 MBit
66 pin
TSOP

16 Pwr/Gnd*
16 Data
15 Addr
7 Cmd
2 Clk *
7 NC *
2 DQS *
1 Vref *
DDR Sdram Chip Architecture

Same basic architecture as SDRAM

Data I/O runs at 2X freq. of DRAM core

Data I/O Interface is different

Same basic architecture as SDRAM

Data I/O runs at 2X freq. of DRAM core

Data I/O Interface is different
Recall: Signal Propagation

Ideal Transmission Line

\[ \sim 0.66c = 20 \text{ cm/ns} \]

PC Board + Module Connectors + Varying Electrical Loads

= Rather non-Ideal Transmission Line
Recall: Clocking Issue

We need different “clocks” for R/W
DQS: Data Strobe

- Topology, electrically matched with signals on data bus
- Source synchronous “clock” signal
- Edge aligned with data for reads, center aligned with data for writes
- Single ended, bidirectional signal in DDR SDRAM memory system
DQS: Read and Write

Read

<table>
<thead>
<tr>
<th>Clk #</th>
<th>Clk</th>
<th>Cmd</th>
<th>DQS</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Read</td>
<td></td>
<td></td>
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</table>

CASL = 2

DQS Pre-amble

DQS Post-amble

Write

<table>
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<th>Data</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>Write</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

DQS Pre-amble

DQS Post-ample
DQS: Read-Read Sequence

DQS pre-amble

DQS post-amble

CASL = 2
Signaling: SSTL-2

- $V_{\text{ref}} = V_{ddq}/2$
- Rail-to-rail swing of 2.5V
DDR SDRAM Quick Summary

- Same basic architecture as SDRAM
- DQS added to better control timing of data transport
- Single-ended, bi-directional DQS signal reduces “efficiency” of access protocol
- Single-ended, bi-directional DQS signal very difficult to turn around on system board level @ 200 MHz
- Data accessed in 2n widths @ frequency m internally and n width @ frequency 2m externally
- Voltage supply dropped to 2.5V, lower power consumption