Memory System Organization

“Mesh Topology”

Single Channel SDRAM Controller

Dimm1, Dimm2, Dimm3, Dimm4

Addr & Cmd
Data Bus
Chip (DIMM) Select
DRAM System Organization

Where is the data?

CPU

Request (Read)
(Physical Address)
(Cacheline length = 64B)

Data

Magic
Memory
Controller

Data

Command
Sequence

Rank Address = ?
Bank Address = ?
Row address = ?
Column Address ?

Rank?
Bank?
Row?
Column?
It’s a “bank” of chips that responds to a single command and returns data.

“Bank” terminology already used.
Rank Part 2

SDRAM
Single Sided Dimm
One Rank

SDRAM
Double Sided Dimm
Two Ranks

Rambus RIMM
Rank Count is
Number of Devices

SDRAM/DDR SDRAM system: 4~6 ranks
RDRAM system: <= 32 ranks
“Banks” of independent memory arrays inside of a DRAM Chip

SDRAM/DDR SDRAM system: 4 banks
RDRAM system: “32” split or 16 full banks
Row and Column Revisited

“Column” Defined

Column: Smallest addressable quantity of DRAM on chip

SDRAM*: column size == chip data bus width (4, 8, 16, 32)
RDRAM: column size != chip data bus width (128 bit fixed)

SDRAM*: get “n” columns per access. n = (1, 2, 4, 8)
RDRAM: get 1 column per access.
Current “PC Class” memory system. 1 physical channel of DDR SDRAM

Intel i850 DRDRAM memory system. 2 physical channel. 1 logical channel

Intel “Granite Bay” memory system. 2 physical channel. 1 logical channel
Channel Part 2

Alpha EV7 DRDRAM memory system
8* physical channels. 2 logical channels

Memory Controller

DRDRAM
DRDRAM
DRDRAM
DRDRAM
DRDRAM
DRDRAM
DRDRAM
DRDRAM
then the data is valid on the data bus ... depending on what you are using for in/out buffers, you might be able to overlap a little or a lot of the data transfer with the next CAS to the same page (this is PAGE MODE).

Address Mapping I

Variable numbers of rank, column, row.
### Address Mapping II

<table>
<thead>
<tr>
<th>Device config</th>
<th>64 Meg x 4</th>
<th>32 Meg x 8</th>
<th>16 Meg x 16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration</td>
<td>16 M x 4 x 4 bks</td>
<td>8 M x 8 x 4 bks</td>
<td>4 M x 16 x 4 bks</td>
</tr>
<tr>
<td>row addressing</td>
<td>8K (A0 - A12)</td>
<td>8K (A0 - A12)</td>
<td>8K (A0 - A12)</td>
</tr>
<tr>
<td>bank addressing</td>
<td>4 (BA0, BA1)</td>
<td>4 (BA0, BA1)</td>
<td>4 (BA0, BA1)</td>
</tr>
<tr>
<td>col addressing</td>
<td>2K(A0-A9,A11)</td>
<td>1K (A0-A9)</td>
<td>512 (A0- A8)</td>
</tr>
</tbody>
</table>

“DRAM page size” differs with different configurations.

8 of the x8 devices form 64 bit wide data bus

4 of the x16 devices form 64 bit wide data bus
then the data is valid on the data bus ... depending on what you are using for in/out buffers, you might be able to overlap a little or a lot of the data transfer with the next CAS to the same page (this is PAGE MODE)

Address Mapping III

32 bit physical address (byte addressable)

no rank row bank column not
memory id id id id used

Device config | 16 Meg x 16
---|---
Configuration | 4 M x 16 x 4 bks
row addressing | 8K (A0 - A12)
bank addressing | 4 (BA0, BA1)
col addressing | 512 (A0 - A8)

One Address Mapping Scheme for 512 MB of Memory
Where’s the data? Part 1

Read Request
Physical Address:
0x0AC75C38

32 bit physical address (byte addressable)

Rank id = 1
Bank id = 1
Row id = 0x0B1D
Column id = 0x187
Where’s the data? Part 2

Rank id = 1
Bank id = 1
Row id = 0x0B1D
Column id = 0x187

FPM / EDO / SDRAM / etc.
Where’s the data? Part 3

Given one column address, SDRAM bursts back “n” beats”, with critical word first.

“n” is programmable. n = 4 for 32 byte cache line. n = 8 for 64 byte cache line.

FPM / EDO / SDRAM / etc.
then the data is valid on the data bus ... depending on what you are using for in/out buffers, you might be able to overlap a little or a lot of the data transfer with the next CAS to the same page (this is PAGE MODE)

Memory Modules I

Bare DIP’s shoved into sockets

Put chips on PCB, make a module

Data

Address

Data

FPM / EDO / SDRAM / etc.
Memory Modules II

Registered DIMM

One extra cycle to buffer and distribute address.

More chips (load) can be placed on module
then the data is valid on the data bus ... depending on what you are using for in/out buffers, you might be able to overlap a little or a lot of the data transfer with the next CAS to the same page (this is PAGE MODE).
SPD: Serial Presence Detect

SPD: Tiny EEPROM
Contains Parameters
- Speed settings
- Configurations
- Programmed by module maker
SDRAM Chip: 54 Pin TSOP

“Same pinout”, except for DQ - data pins
Kingston SDRAM DIMM

8 Chips. 128 Mbit each. (Infineon) SPD

PC133 CAS 3

Dual Inline Memory Module