Intel 875P Chipset

- Intel® Pentium® 4 Processor
- DDR400/333 SDRAM
- 6.4, 4.2 or 3.2 GB/s
- AGP8X
  - 2.0 GB/s
- Communication Streaming Architecture/GbE
- 82875P MCH
- Intel® Hub Architecture
- DDR
  - 6.4 GB/s
- DDR
- 8 Channel Audio
  - 133 MB/s
- PCI
  - Hi-Speed USB 2.0
  - 8 Ports
- BIOS Supports HT Technology
- Intel® RAID Technology (ICH5R only)
- Dual Independent Serial ATA Ports
- 150 MB/s
- 10/100 LAN Connect Interface
- Legacy ATA 100
CPU-Chipset Interface I (FSB)

Arbitrate

Request

Response

Snoop

5 Load Multi-drop Pentium Pro Bus Protocol

- Glueless multiprocessor, up to 4 CPU’s
- Multiple signal groups. “Owner” controls signal group for that “phase”
- Protocol initially operated @ 66 MHz
The “cycle time” of the interconnect must account for symbol transport time as well as bus interface logic cycle time.
CPU-Chipset Interface III

- Base Freq
- Address strobe
- Host data strobe (differential)

One “Cycle”

Pseudo Point to point

I/O Buffer
CPU-Chipset Interface IV

Data Bus width: 64 bits

@ 100 MHz - 400 Mpbs = 3.2 GB/s
@ 133 MHz - 533 Mpbs = 4.2 GB/s
@ 200 MHz - 800 Mpbs = 6.4 GB/s
CPU-Chipset Interface V

Dynamic Bus Inversion

- Terminating resistor supplies “1”, voltage on bus is equal to Vddq when no driver is active
- Driver sinks current to Vssq when it needs to drive “0”
- Power consumed when “driving 0” and active current sinks
- One extra signal per 16 data signals to signify whether those 16 signals are inverted or not. Maximum of 8 signals “driven to 0” per 16 signal group
“Dual Channel” DDR SDRAM

- 133 MHz (266 Mbps, 2.1 GB/s PC2100)
- 167 MHz (333 Mbps, 2.7 GB/s PC2700)
- 200 MHz (400 Mbps, 3.2 GB/s PC3200)
Single vs Dual Channel Mode

Single Channel Mode: up to 3.2 GB/s
Dual Channel Mode: up to 6.4 GB/s
Multiple Clock Domains I

<table>
<thead>
<tr>
<th>Host Clock</th>
<th>Dram Clock</th>
<th>Ratios</th>
<th>Peak BW</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 MHz</td>
<td>133 MHz</td>
<td>3:4</td>
<td>2.1 GB/s</td>
</tr>
<tr>
<td>133 MHz</td>
<td>133 MHz</td>
<td>1:1</td>
<td>2.1 GB/s</td>
</tr>
<tr>
<td>200 MHz</td>
<td>133 MHz</td>
<td>3:2</td>
<td>2.1 GB/s</td>
</tr>
<tr>
<td>133 MHz</td>
<td>166 MHz</td>
<td>4:5</td>
<td>2.7 GB/s</td>
</tr>
<tr>
<td>200 MHz</td>
<td>160 MHz</td>
<td>5:4</td>
<td>2.6 GB/s</td>
</tr>
<tr>
<td>200 MHz</td>
<td>200 MHz</td>
<td>1:1</td>
<td>3.2 GB/s</td>
</tr>
</tbody>
</table>
Multiple Clock Domains II

Figure 14. Intel® 875P Chipset System Clock Block Diagram

- Most clock networks in system use spread spectrum
- Basic Idea: Register space in controller records size of memory in each rank.

DRB0: Memory in "row 0" (64 MB increment)
DRB1: Memory in "row 0" + "row 1" (64 MB increment)
DRB2: Memory in "row 0" + "row 1" + "row 2"
   etc. etc.
DRAM “Row” Attribute Registers

<table>
<thead>
<tr>
<th>Device config</th>
<th>32 Meg x 8</th>
<th>16 Meg x 16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration</td>
<td>8 M x 8 x 4 bks</td>
<td>4 M x 16 x 4 bks</td>
</tr>
<tr>
<td>row addressing</td>
<td>8K (A0 - A12)</td>
<td>8K (A0 - A12)</td>
</tr>
<tr>
<td>bank addressing</td>
<td>4 (BA0, BA1)</td>
<td>4 (BA0, BA1)</td>
</tr>
<tr>
<td>col addressing</td>
<td>1K (A0-A9)</td>
<td>512 (A0- A8)</td>
</tr>
</tbody>
</table>

- Basic Idea: Register space in controller records “page size” of memory in each “row” (rank)
- Assists in breaking down physical address into row/column addresses
- Page sizes are 4KB, 8KB, 16KB and 32KB
DRAM Timing Registers

- Basic Idea: Register space in controller records timing parameters of DRAM

- tRAS, tPR, tRCD, tCL

- Memory controller must know everything about configuration and state of DRAM memory system

Case 1: Memory access is to location not already contained in row buffer. Requires a row access followed by a column access.

Case 2: Memory access is to location already contained in row buffer. Requires only a column access.

Case 3: Memory access is to location not in row buffer, row buffer contains data, precharge needed. (Bank Conflict) Requires a precharge, followed by a row access, followed by a column access.
Advanced Graphics Port 3.0

- Chipset implements backward compatible mode with AGP 2.0 mode
- Supports AGP 8X and 4X modes
- 32 bit (4 byte) databus width @ 533 Mbps = 2.1 GB/s peak data rate
- Dynamic Bus Inversion: New to AGP 3.0
- Calibration cycle required
- Voltage swing 0.8V (Vref = 0.35V)
CSA/GbE

- “Communication Streaming Architecture” targeted for GigaBit Ethernet
- 8 bit databus width @ 266 Mbps = 266 MB/s peak data rate hub interface
- Voltage swing 1.5V
Serial ATA

- Serial differential point to point interconnect
- 100 Ohm (differential) matched termination at receiver
- 1.5 Gb/s raw data rate, 8/10 embedded clock encoding, 1.2 Gb/s (150 MB/s) usable peak data rate
- Migration path to 3.0/2.4 Gb/s data rate in mid 2004
- Cost competitive with Ultra ATA infrastructure
- emulate existing (parallel) ATA Master/Slave architecture