DRAM For Embedded Systems:

FCRAM, RLDRAM, Rambus Yellowstone, NetDDR

Diagram showing DRAM technologies with axes for "Faster" DRAM Cores and Higher Data Rate Interface, leading to "Yellowstone" with higher performance.
DRAM for Embedded Systems

- Relatively small memory size demand. Tens of megabytes. One or two chips would provide sufficient capacity.
- No need for expandability (one/two ranks), no need for sockets, short traces.
- Examples: Graphics cards, network routers, Sony Playstation.
- Low(er) latency, High(er) cost.
- Diverse requirements. Graphics cards favor streaming. Network equipment favors random access of 40 byte (IP) packets or 53 byte (ATM) packets.
Rambus Yellowstone:

Next Generation Memory Signalling Technology from Rambus

DRSL: Differential Rambus Signaling Level
ODR: Octal Data Rate
FlexPhase: Per bit de-skewing by controller
Yellowstone Features

- 3.2 Gbps data rate
- Low Voltage Differential Signalling
- Per bit deskewing control eliminates necessity for path length matching
- Implementable on commodity 4 layer PCB with standard design rules
- No connector specification (for embedded systems)
Yellowstone Topology:

- Low chip count, high bandwidth DRAM memory system
Yellowstone DRSL Signaling:

- Data bits are transported by differential, point to point low voltage signals. Differential Rambus Signaling Levels
Yellowstone ODR Clocking:

3.2 Gbps Data Rate

400 MHz reference clock signal

Octal Data Rate
Yellowstone FlexPhase:

FlexPhase: Per bit deskewing circuit

FlexPhase

3.2 Gbps Data Rate

latch

PLL

FlexPhase

3.2 Gbps Data Rate

latch

DRAM Controller

DRAM Chip
Yellowstone Channel Routing

- Address/Command Bus signals are path length matched (800 Mbps)
- Flexphase makes it unnecessary to path length match data signals (3.2 Gbps)
## FCRAM

**Fast Cycle RAM (aka Network-DRAM)**

<table>
<thead>
<tr>
<th>Features</th>
<th>DDR SDRAM</th>
<th>FCRAM/Network-DRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd, Vddq</td>
<td>2.5 +/- 0.2V</td>
<td>2.5 +/- 0.15</td>
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<tr>
<td>Electrical Interface</td>
<td>SSTL-2</td>
<td>SSTL-2</td>
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<tr>
<td>Clock Frequency</td>
<td>100~167 MHz</td>
<td>154~200 MHz</td>
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<tr>
<td>t_{RAC}</td>
<td>~40ns</td>
<td>22~26ns</td>
</tr>
<tr>
<td>t_{RC}</td>
<td>~60ns</td>
<td>25~30ns</td>
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<tr>
<td># Banks</td>
<td>4</td>
<td>4</td>
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<tr>
<td>Burst Length</td>
<td>2,4,8</td>
<td>2,4</td>
</tr>
<tr>
<td>Write Latency</td>
<td>1 Clock</td>
<td>CASL -1</td>
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</table>

FCRAM/Network-DRAM looks like DDR+  
*Can share controller with DDR SDRAM*
Faster $t_{RC}$ allows Samsung to claim higher bus efficiency

* Samsung Electronics, Denali MemCon 2002
Another Variant, but RLDRAM is targeted toward embedded systems. There are no connector specifications, so it can target a higher frequency off the bat.

<table>
<thead>
<tr>
<th>DRAM Type</th>
<th>Frequency (data rate)</th>
<th>Bus Width (per chip)</th>
<th>Peak Bandwidth (per Chip)</th>
<th>Random Access Time (t&lt;sub&gt;RAC&lt;/sub&gt;)</th>
<th>Row Cycle Time (t&lt;sub&gt;RC&lt;/sub&gt;)</th>
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<tbody>
<tr>
<td>PC133 SDRAM</td>
<td>133</td>
<td>16</td>
<td>266 MB/s</td>
<td>45 ns</td>
<td>60 ns</td>
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<td>DDR 200</td>
<td>200 * 2</td>
<td>16</td>
<td>0.8 GB/s</td>
<td>30 ns</td>
<td>55 ns</td>
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<td>PC800 RDRAM</td>
<td>400 * 2</td>
<td>16</td>
<td>1.6 GB/s</td>
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<td>70 ns</td>
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<td>FCRAM</td>
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<td>25 ns</td>
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<tr>
<td>RLDRAI I</td>
<td>300 * 2</td>
<td>32</td>
<td>2.4 GB/s</td>
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<td>25 ns</td>
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<tr>
<td>RLDRAII</td>
<td>400 * 2</td>
<td>36</td>
<td>3.6 GB/s</td>
<td>20 ns</td>
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</table>

Comparable to FCRAM in latency
Higher Frequency (No Connectors)
non-Multiplexed Address (SRAM like)
RLDRAM is a great replacement to SRAM in L3 cache applications because of its high density, low power and low cost.

* Infineon Presentation, Denali MemCon 2002
Quad Band Memory

Uses Fet switches to control which DIMM sends output. Two DDR memory chips are interleaved to get Quad memory. Does not improve efficiency, but cheap bandwidth. Supports more loads than "ordinary DDR", so more capacity.

"Wrapper Electronics around DDR memory"
Generates 4 data bits per cycle instead of 2.

Quad Band Memory
DDR ESDRAM Part I

“Single Transistor SRAM”
300 MHz, 600 mbps data rate
Always - close page - policy
16 Banks Internally
Deassert - Hidden Refresh
Read or Write Latency of 4 or 6 cycles
Fixed Burst Length of 8 beats

Accesses to alternate banks can be fully pipelined
Next generation HP PA-RISC “Mako” processor
Use 4 chips to form 32 MB ECC protected L2 DRAM cache

Accesses to same banks cannot be fully pipelined
DDR ESDRAM Part III

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<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
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<th>F</th>
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<td>DQ</td>
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</table>

“Clamshell” pinout

DDR ESDRAM

“Top”

PCB Board

“Bottom”
eDRAM

Available in pre-constructed Macros
May be available in varying widths (292 now, 1168 later)
Fast row cycle time (sub 10ns)
Fast access time (5 to 13 ns)
Targetted toward speed or density
Pushing to replace SRAM for cache (4X denser)

![Diagram]

Intel 0.13um silicon - “Northwood” ~ 140mm^2 ~ ASP $150
AMD 0.13um silicon - Athlon ~ 100 mm^2 ~ ASP $80
DRAM 0.13um silicon - various ~ 60 mm^2 ~ ASP $3~4
Embedded DRAM Primer

Embedded

Not Embedded
Whither Embedded DRAM?


- Two predict imminent merger of CPU and DRAM
- Another states we cannot keep cramming more data over the pins at faster rates (implication: embedded DRAM)
- A fourth wants gigantic on-chip L3 cache (perhaps DRAM L3 implementation?)

SO WHAT HAPPENED?
Whither Embedded DRAM? II

- MoSys and Atmos have planer designs announced (integrates easily into logic flow)
- IBM pushing trench design but make it attractive
- IBM’s tRC=12ns @ 130nm and 5ns @ 100nm matches all but fastest SRAM, 40% space overhead
- Soft error rate much lower than for SRAM
- eDRAM’s bandwidth specs match DSP just as easily as vector... DSP much better understood