DDR II Memory System

Same Topology as SDRAM & DDR SDRAM

Addr & Cmd
Data Bus
Differential DQS
Chip (DIMM) Select
DDR II SDRAM Chip Basics

200, 266, 333 MHz $f_{ck}$ (400, 533, 667 Mbps)

Multiplexed Address Bus

Programmable Burst Length 4, 8

Quad Banks Internally (1+ Gb: 8 banks)

Read Latency, CAS = 3, 4, 5

Write Latency, WL = CL - 1

Posted CAS

Additive Latency, AL = 0, 1, 2, 3, 4, 5

Differential Data Strobe

Supply Voltage of 1.8V (2.5V optional)

SSTL_18 Signaling ($0.5*V_{ddq}^{\pm} \pm 0.1V$)

(0 to 1.8V rail to rail.)

Programmable I/O Drive Strength

On Die Termination
DDR II Chip Architecture

Same basic architecture as SDRAM & DDR SDRAM (+Hardware for Posted CAS)
Data I/O runs at 4X bit rate of DRAM core

Data I/O Interface is different

ODT control clk OCD control

Data bus (and mask)

DQS
Recall: “DRAM Evolution”

<table>
<thead>
<tr>
<th>Year</th>
<th>DRAM Generation</th>
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<tbody>
<tr>
<td>1995</td>
<td>16Mbit</td>
</tr>
<tr>
<td>1998</td>
<td>64Mbit</td>
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<tr>
<td>2001</td>
<td>256Mbit</td>
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<tr>
<td>2004</td>
<td>1Gbit</td>
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</tbody>
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Internal datapath width (16 bit external I/O)

- DDR SDRAM: 200 Mbp/s/p
- SDRAM: 100 Mbp/s/p
- DDR: 400 Mbp/s/p
- SDRAM: 800 Mbp/s/p
- {DDR2}: {RDRAM}
- SLDRAM: >1 Gbp/s/p

Cost adder: 5%
Mode Registers

SDRAM, DDR SDRAM & DDR II SDRAM Devices can be programmed to behave in slightly different manners.
Posted CAS (Read)

CAS command follows RAS command. (AL = 0)

1. RAS: Row Access
2. CAS: Column Read Access
Posted CAS (Write)

CAS Write follows RAS. \((t_{AL} = 0, t_{WL} = 2)\)

1. RAS: Row Access
2. CAS: Column Write Access

\(t_{AL} \) (Additive Latency) \(t_{WL} = t_{CAS} + t_{AL} - 1\)
Write after Read (same rank)

1. RAS: Row Access
2. CAS: Column Read Command
3. CAS: Column Read Data
4. CAS: Column Write Command
5. CAS: Column Write Data

$t_{RL} = t_{CAS} + t_{AL} = 3 + 2 = 5$
$t_{WL} = t_{CAS} + t_{AL} - 1 = t_{RL} - 1 = 4$
Read after Write (same rank)

1. RAS: Row Access
2. CAS: Column Write Command
3. CAS: Column Write Data
4. CAS: Column Read Command
5. CAS: Column Read Data

\[ t_{RL} = t_{CAS} + t_{AL} = 3 + 2 = 5 \]
\[ t_{WL} = t_{CAS} + t_{AL} - 1 = t_{RL} - 1 = 4 \]
Recall: DQS in DDR SDRAM

- Topology, electrically matched with signals on data bus
- Source synchronous “clock” signal
- Edge aligned with data for reads, center aligned with data for writes
- Single ended, bidirectional signal in DDR SDRAM memory system
- One signal per byte
DQS in DDR II

- Topology, electrically matched with signals on data bus
- Source synchronous “clock” signal
- Edge aligned with data for reads, center aligned with data for writes
- **Differential**, bidirectional signal in DDR II memory system
Signaling: SSTL-18

- $V_{\text{ref}} = V_{\text{ddq}}/2$
- Rail-to-rail swing of 1.8V

$V_{\text{in}} \text{ low} = V_{\text{ref}} - 0.125v$
$V_{\text{in}} \text{ High} = V_{\text{ref}} + 0.125v$

$V_{\text{out}} \text{ hi} = V_{\text{tt}} + 0.603V$
$V_{\text{out}} \text{ low} = V_{\text{tt}} - 0.603V$
Impedance Topology I

-Recall: If

\[ Z_{\text{out}} \ll Z_0, \text{ voltage mode} \]

\[ Z_{\text{out}} \gg Z_0, \text{ current mode.} \]
Impedance Topology II

Write

Controller

Read

Controller
ODT: On Die Termination

- Controlled by memory controller via ODT pin.
- Can be turned on/off in 2 cycles
- Provides active termination at the receiver interface.
ODT Control for Read

- **ck#**: Clock enable signal
- **ck**: Clock signal
- **cmd**: Command signal
- **data**: Data signal
- **dqs#**: Data strobe enable signal
- **dqs**: Data strobe signal
- **ODT**: Open Drain Tri-state buffer
- **Rtt (controller)**: Runt time (controller)
- **Rtt (DRAM)**: Runt time (DRAM)

- **to slot 1**: Data transfer to slot 1
- **to slot 2**: Data transfer to slot 2

- **ODT turn on delay**: Delay for turning on ODT
- **ODT turn off delay**: Delay for turning off ODT

- **Controller**: Control signals
- **Z out**: Output termination
- **Z_0**: Zero termination

- **Z_0 -> terminate**: Terminate output signal
DDR II Quick Summary

- Same basic architecture as DDR SDRAM
- Optional DQS and RDQS (RDQS) added to better control timing of data transport
- Data accessed in 4n widths @ frequency m internally and n width @ frequency 4m externally
- DRAM Core and I/O voltage supplies dropped to 1.8V, 2.5V retained in spec for use with DDR SDRAM compliant system designs
- Dynamic termination control
- Edge rate calibration/control