Basics

DRAM ORGANIZATION

- Storage element (capacitor)
- Word Line
- Bit Line
- Switching element
- Data In/Out Buffers
- Sense Amps
- Column Decoder
- Memory Array
- Row Decoder
- ... Bit Lines...
- ... Word Lines...
Basics

BUS TRANSMISSION

CPU

MEMORY CONTROLLER

BUS

DRAM

Row Decoder

Data In/Out Buffers

Sense Amps

Column Decoder

... Bit Lines...

Memory Array

... Word Lines...
Basics

[PRECHARGE and] ROW ACCESS

AKA: OPEN a DRAM Page/Row
     or
ACT (Activate a DRAM Page/Row)
     or
RAS (Row Address Strobe)
Basics

COLUMN ACCESS

READ Command
or
CAS: Column Address Strobe
Basics

DATA TRANSFER

note: page mode enables overlap with CAS

... with optional additional
CAS: Column Address Strobe
Basics

BUS TRANSMISSION

- CPU
- MEMORY CONTROLLER
- BUS
- DRAM
- Column Decoder
- Sense Amps
- ... Bit Lines...
- Row Decoder
- Word Lines...
- Memory Array
- Data In/Out Buffers

... Bit Lines...
Basics

A: Transaction request may be delayed in Queue
B: Transaction request sent to Memory Controller
C: Transaction converted to Command Sequences (may be queued)

D: Command/s Sent to DRAM
E_1: Requires only a CAS or
E_2: Requires RAS + CAS or
E_3: Requires PRE + RAS + CAS
F: Transaction sent back to CPU

“DRAM Latency” = A + B + C + D + E + F
Basics

Read Timing for Conventional DRAM

![Diagram of Read Timing for Conventional DRAM](image)

- **RAS** (Row Address Select)
- **CAS** (Column Address Select)
- **Address**
- **DQ** (Data Out)
- **Valid Dataout**
- **Row Access**
- **Column Access**
- **Data Transfer**
DRAM Evolutionary Tree

(Mostly) Structural Modifications
Targeting Throughput

FPM → EDO → P/BEDO → SDRAM → ESDRAM → VCDRAM → FCRAM → MOSYS

Structural Modifications
Targeting Latency

Interface Modifications
Targeting Throughput

Rambus, DDR/2 → Future Trends

Conventional DRAM

Targeting Throughput
DRAM Evolution

Read Timing for Conventional DRAM

Row Access
Column Access
Transfer Overlap
Data Transfer

Row Address
Column Address
Valid Dataout

RAS
CAS
Address
DQ
Row Address
Column Address
Row Address
Column Address
Valid Dataout
DRAM Evolution

Read Timing for Fast Page Mode

- RAS
- CAS
- Address
- Column Address
- Valid Dataout
- Data Transfer
- Column Access
- Transfer Overlap
- Row Access
DRAM Evolution

Read Timing for Extended Data Out

Row Access
Column Access
Transfer Overlap
Data Transfer

RAS
CAS
Address
Row Address
Column Address
Column Address
Column Address
DQ
Valid Dataout
Valid Dataout
Valid Dataout

Data Transfer
Column Access
Row Access
DRAM Evolution

Read Timing for Burst EDO

![Diagram of DRAM timing](image-url)
DRAM Evolution

Read Timing for Pipeline Burst EDO

- Row Access
- Column Access
- Transfer Overlap
- Data Transfer

Diagram showing the timing of row and column accesses, along with data transfer and overlap.
DRAM Evolution

Read Timing for Synchronous DRAM

(RAS + CAS + OE ... == Command Bus)
DRAM Evolution

Inter-Row Read Timing for ESDRAM

Regular CAS-2 SDRAM, R/R to same bank

ESDRAM, R/R to same bank
DRAM Evolution

Write-Around in ESDRAM

Regular CAS-2 SDRAM, R/W/R to same bank, rows 0/1/0

ESDRAM, R/W/R to same bank, rows 0/1/0

(can second READ be this aggressive?)
DRAM Evolution

Internal Structure of Virtual Channel

Segment cache is software-managed, reduces energy
DRAM Evolution

Internal Structure of Fast Cycle RAM

- **SDRAM**
  - 8M Array (8Kx 1Kb)
  - Sense Amps
  - $t_{RCD} = 15\text{ns}$ (two clocks)

- **FCRAM**
  - 8M Array (?)
  - Sense Amps
  - $t_{RCD} = 5\text{ns}$ (one clock)

Reduces access time and energy/access
DRAM Evolution

Internal Structure of MoSys 1T-SRAM

addr
Bank Select
Auto Refresh
$ DQs
## DRAM Evolution

### Comparison of Low-Latency DRAM Cores

<table>
<thead>
<tr>
<th>DRAM Type</th>
<th>Data Bus Speed</th>
<th>Bus Width (per chip)</th>
<th>Peak BW (per Chip)</th>
<th>RAS–CAS (t_{RCD})</th>
<th>RAS–DQ (t_{RAC})</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC133 SDRAM</td>
<td>133</td>
<td>16</td>
<td>266 MB/s</td>
<td>15 ns</td>
<td>30 ns</td>
</tr>
<tr>
<td>ESDRAM</td>
<td>166</td>
<td>16</td>
<td>332 MB/s</td>
<td>12 ns</td>
<td>24 ns</td>
</tr>
<tr>
<td>VCDRAM</td>
<td>133</td>
<td>16</td>
<td>266 MB/s</td>
<td>30 ns</td>
<td>45 ns</td>
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<tr>
<td>FCRAM</td>
<td>200 * 2</td>
<td>16</td>
<td>800 MB/s</td>
<td>5 ns</td>
<td>22 ns</td>
</tr>
<tr>
<td>1T-SRAM</td>
<td>200</td>
<td>32</td>
<td>800 MB/s</td>
<td>—</td>
<td>10 ns</td>
</tr>
<tr>
<td>DDR 266</td>
<td>133 * 2</td>
<td>16</td>
<td>532 MB/s</td>
<td>20 ns</td>
<td>45 ns</td>
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<tr>
<td>DRDRAM</td>
<td>400 * 2</td>
<td>16</td>
<td>1.6 GB/s</td>
<td>22.5 ns</td>
<td>60 ns</td>
</tr>
<tr>
<td>RLDRAM</td>
<td>300 * 2</td>
<td>32</td>
<td>2.4 GB/s</td>
<td>???</td>
<td>25 ns</td>
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