1. Basic Information

Time and Place
Lecture: TuTh 6:30pm – 7:45pm, CHE 2136

Professor
Peter Petrov, AVW-1421, ppetrov@ece.umd.edu
Office hours: Open doors and email appointment


2. Course Overview
This course covers fundamental and advanced concepts in modern computer architecture. Instruction level parallelism (ILP) and its exploitation, including pipelining, branch prediction, dynamic scheduling, speculation, multiple-issue engines, VLIW architectures, ILP limits. The memory hierarchy design will be covered in details by focusing on more advanced cache organizations/optimizations and support for virtual memory and virtual machines. One of the major focuses of the class would be the thread-level and data-level parallelism and its exploitation by multiprocessors. We will cover symmetric and distributed shared-memory multiprocessor organizations and the related issues of synchronization, consistency and coherence.

3. Prerequisites
You should have taken an undergraduate course in computer architecture, i.e. ENEE 446. This course will build upon fundamental knowledge of digital logic design and computer organization.

4. Course Material
There is one required textbook for the course. We may also discuss material in research papers, which will be posted on the class web page.


5. Course Work, Policies, and Grading
There will be 2 (two) midterm exams and a final exam. The exams will be based entirely on the course readings and will be closed book, closed notes. Before each exam I will assign practice problems, which sole purpose will be to prepare you for the exams. The practice problems will be neither collected, nor graded. The final grade will be formed as follows:

Midterm 1 (in class) : 30%
Midterm 2 (in class) : 30%
Final : 40%

6. Special Needs
If you have a documented disability that requires special needs, please see me as soon as possible.