1. Bulk Silicon Materials
   a. Consider the diode structure shown below. Calculate the anode (n$^+$-side) and cathode (p-side) parasitic resistances near the “cut-in” voltage. (20pts)
   b. What is the parasitic capacitance at 5V reverse bias? (10pts)
   c. Describe an iterative technique for finding the diode drop in the circuit shown on the next page. (10pts)

2. Process Technology
   a. Provide a process flow for a simple n+/p diode. Be sure to show the completed structure in cross section and in plan-view. (15pts)
   b. What factors must you take into account to create a “minimum area” component? What factors must you take into account in placing two of these components together side-by-side? (15pts)
3. Space Charge

   a. Using the Fermi No-droop Theorem, what is the mobile charge density at the
      metallurgical junction of the diode described in problem 1. You may take the forward bias
      to be 0.7V.? (15pts)

   b. Estimate the electric field in the p-side quasi-neutral region? (15pts)