1a. By “p-side and n-side parasitics” the question referred to physical resistances due to undepleted material. Some class responses took this to mean the diode forward resistance (from the small signal model). I accepted this approach as well. But you had to find a way to estimate the forward drop across the diode. Let’s work out the physical resistances first. This is a bit numerically intensive. First, work out the built in potential:

\[ \phi_{bi} = 0.0259 \ln \left( \frac{10^{18} \times 10^{16}}{(1.45 \times 10^{10})^2} \right) = 0.82V \]  \hspace{1cm} (1)

Near cut-in, the space charge thickness is close to the unbiased thickness:

\[ x_{sc} = \sqrt{\frac{2\epsilon_{si}(N_a + N_d)}{q(N_aN_d)(\phi_{bi})}} = \sqrt{10^{-9}} = 0.32\mu m \]  \hspace{1cm} (2)

Only about one-hundredth of this penetrates into the n+ layer, so the transport distance of the \( R_n \) parasitic is the full 2 microns. The full space charge thickness is much less than 200\( \mu \)m, so the space charge doesn’t really figure in to the resistance calculations at all! (But you must perform some evaluation to state this with certainty.) From the “formulary” (i.e., cheat sheet),

\[ R_n = \rho G = \frac{1}{eN_d\mu} \frac{2 \times 10^{-4}}{1.2^2} \]  \hspace{1cm} (3)

\[ R_n = \frac{1}{1.6 \times 10^{-19} \times 10^{18} \times 1.5 \times 10^3 \times 2 \times 10^{-2}} = 4.8 \times 10^{-4} \]  \hspace{1cm} (4)

or 0.48milliOhm. and

\[ R_p = \rho G = \frac{1}{eN_a\mu} \frac{2 \times 10^{-2}}{1.2^2} \]  \hspace{1cm} (5)

\[ R_p = \frac{1}{1.6 \times 10^{-19} \times 10^{16} \times 0.5 \times 10^3 \times 2} = \frac{2}{0.8} = 2.5\Omega \]  \hspace{1cm} (6)

Now consider the diode forward resistance. Here, the relevant equations are:
\[ I_d = I_s \exp \left( \frac{qV_a}{kT} \right) - 1 \]  
(7)

\[ r_d = \left( \frac{\partial I_d}{\partial V_a} \right)^{-1} = \left[ \frac{qI_s}{kT} \exp \left( \frac{qV_a}{kT} \right) \right]^{-1} \approx \frac{V_t}{I_d} \]  
(8)

where \( V_t \) is the “thermal” voltage (0.0259V). From the solution to 1c (below), we know that a good estimate of \( I_d \) is 4.2mA. Thus:

\[ r_d = \frac{0.0259}{4.2 \times 10^{-3}} = 6.2\Omega \]  
(9)

and, as it turns out, this is the dominant forward resistance. 1b. In reverse bias, the only parasitic capacitance is the depletion capacitance:

\[ C_{sc} = \frac{A\epsilon_{si}}{x_{sc}} \]  
(10)

and we know that:

\[ x_{sc} = \sqrt{\frac{2\epsilon_{si}(N_a + N_d)}{q(N_aN_d)}}(\phi_{bi} - V_a) \]  
(11)

Thus:

\[ x_{sc} = \sqrt{\frac{2 \times 10^{-12} \times 5.8}{1.6 \times 10^{-19} \times 10^{16}}} = 0.85\mu m \]  
(12)

and:

\[ C_{sc} = \frac{A\epsilon_{si}}{x_{sc}} = \frac{0.01 \times 10^{-12}}{0.85 \times 10^{-14}} = 1.2 \times 10^{-10} \]  
(13)

or 0.12nF.

1c. Here’s a nifty way to solve this. First assume that there’s an 0.8 V drop across the whole of the diode. As we showed above, we can neglect the \( R_n, R_p \) parasitics as they’re much less than the series resistance. Thus, the drop across the resistor is 5 - 0.8 = 4.2 volts, and the resistor-limited current is 4.2mA. Next we can up-date our guess at the diode drop:

\[ V_a = \frac{kT}{q} \ln\left[ \frac{I_d}{I_s} - 1 \right] \]  
(14)

We subtract that new drop estimate from the supply voltage, divide by the resistance, use hat for \( I_d \) and do the dance again. I include a few iterates below (even though I didn’t expect you to do this in the exam.

2a. Here is the flow and the plane-view for the diode:

2b. There are four elements that should be considered when discussing density of components:
1. Clean and oxidize silicon surface
2. Deposit photoresist
3. Create mask aperture using photolithography
4. Etch aperture in oxide
5. Implant n+ layer
6. Strip old photoresist
7. Re-spin new resist
8. Implant p+ contacts
9. Strip old resist
10. Deposit metal
11. Re-spin new resist
12. Expose and develop photoresist
13. Etch metal
14. Strip photoresist -→ DONE!

PROCESS FLOW AND PLANE-VIEW OF DIODE STRUCTURE
• Lithographic Resolution
• Overlap of Space Charge Regions
• Breakdown Voltages
• Power Density

The lithographic resolution defines the minimum resolvable feature size. For an optical “stepper,” this resolution is given by:

\[ x_{\text{min}} = \frac{k_1 \lambda}{NA} \]  

where \( k_1 \) is processing constant (basically, a “fudge” factor), \( \lambda \) is the wavelength of the exposing light, and \( NA \) is the numerical aperture of the lens system. Surprisingly, that doesn’t really influence the diode size. The smallest feature, in my design, is the central contact window. But the diffusions balloon around that central region and define the component size. In any event, it should be noted that there are really two resolution issues: the minimum resolved feature size (which differs for different materials, even if you keep the litho tool the same), and the minimum feature spacing. The formula I provided for minimum line and space dimensions \( (d_{\text{min}} = 1.25\sqrt{g}) \), does provide that information. But note, it is for a contact printer!

As two diffusions of the same sign (and of opposite sign to the substrate) get closer together, the potential barrier between the two diffused regions start to overlap and the barrier starts to get smaller. This means that the isolating fields between the regions go to zero, and the diffusions aren’t distinct. This sets a minimum close approach distance between two n+ regions. This isn’t too much of a problem here, as we have a kind of p+ guard-ring surround to the n+ layer.

You should also estimate the maximum current drawn by a component and multiply this by the maximum bias drop across the component. This gives the power dissipation for the device, \( P \). If we make an array of such devices with \( N \) units, the power dissipated by the \( N \) units will be \( NP \). Divide that by the array area will give the power density of the array. Every chip has a maximum allowable density which must not be exceeded. Spreading the devices out lowers this density.

As two n+ and p+ diffusions start to overlap, the built in field and the field-under-bias between the two features goes up significantly. This creates a breakdown limit for spacing the metallurgical junctions between these two diffusion tubs. You can’t strictly call this space charge overlap, since there us no space charge associated with the heavily doped layer the same sign as the substrate.

3a. Begin by considering the band-edge vs position diagram shown below.

As we discussed in class, at the space charge edges, The minority charge densities are elevated by a factor an exponential factor. The electron minority density on the p-side, at the space charge edge, is:
This is because the electron Fermi level has been elevated over its equilibrium level (pushed closer to the conduction band edge) by an amount equal to $V_a$. Inspection of the diagram indicates that the electron Fermi level (assuming no-droop) is $V_a/2$ higher than mid-gap. Thus, the non-equilibrium electron (and hole!) concentration at the metallurgical junction is:

$$n = n_i \exp(\frac{qV_a}{kT}) = 1.45 \times 10^{10} \exp(38.61 \times .41) = 1.1 \times 10^{17}$$

(17)

Also, please note that we have taken the whole cut-in bias as occurring across the metallurgical junction. This does not include the fact that the current creates drops across the $R_p$ and $R_n$ parasitics. This added factor can be included iteratively (as in the diode drop model described above). 2b. As always;

$$j = \sigma E$$

(18)

or:

$$E = \frac{j}{\sigma} = \frac{I_d}{qN_a\mu_p A}$$

(19)

From data presented (or derived):

$$E = \frac{1}{1.6 \times 10^{-19} \times 10^{16} \times 5 \times 10^2} \times \frac{4.2 \times 10^{-3}}{.01} = 0.52 V/cm$$

(20)
It’s very low, but the background density is high, so you don’t need a lot of field to push a substantial amount of charge around.