MOSFETs

1. Thermal energy carries the mobile charges “up-hill” into the bulk. The mean kinetic energy gets converted to potential in the up-hill move. Even though the space charge potential is parabolic as a function of distance, my hint suggested that you just look near the surface where the field looks constant and the potential vs distance diagram is linear. This simplifies things a bit, as you can see from the figure below:

![Diagram of potential vs position near the oxide/semiconductor interface and the relationship of this variation to “classical” inversion thickness.]

Figure 1: Potential vs position near the oxide/semiconductor interface and the relationship of this variation to “classical” inversion thickness.

So, first we find E. We know from Gauss’ law that:

\[ E = \frac{\sigma}{\epsilon_{si}} \]  

(1)
where $\sigma$ and $\epsilon_{si}$ are the sheet charge in the space charge and dielectric permittivity of silicon, respectively. We calculate the sheet charge density as follows:

$$\sigma = qN_a x_{sc} = qN_a \sqrt{\frac{2\epsilon_{si}2\phi_b}{qN_a}} = \sqrt{qN_a2\epsilon_{si}2\phi_b} = 6.7 \times 10^{-8} \text{C/cm}^2$$

To get the field, we divide this by the silicon dielectric permittivity to get: $E = 6.7 \times 10^4 \text{V/cm}$. The kinetic energy of the carriers is gotten from the equipartition theorem:

$$E_{ke} = \frac{3}{2} kT = 1.5 \times 8.62 \times 10^{-5}\text{300} = .04 \text{eV}$$

And now we can solve:

$$E_{ke} = \frac{3}{2} kT = E_{x_{inv}}$$

which yields: $x_{inv} = 58 \, \text{Å}$. This is a bit big. Actually, as we were only considering the 1 degree of freedom (normal to the oxide semiconductor interface) we probably should have used $\frac{1}{2} kT$, yielding $x_{inv} = 19\, \text{Å}$- a value which coincides well with the quantum mechanical value!

2a. The “intrinsic” threshold voltage is:

$$V_{th}^0 = 2\phi_b + \frac{1}{C_{ox}} \sqrt{qN_a2\epsilon_{si}2\phi_b}$$

where:

$$\phi_b = \frac{kT}{q} \ln \left[ \frac{N_a}{n_i} \right]$$

$$C_{ox} = \frac{\epsilon_{si}}{d_{ox}}$$

for the conditions listed, $\phi_b = 0.35\, \text{V}$ and $C_{ox} = 3.45 \times 10^{-7} \text{F/d/cm}^2$ yielding $V_{th}^0 = 0.84\, \text{V}$. The Fermi level of the metal is above that of the semiconductor prior to equilibrium. Equilibrium is achieved by transfer of electrons from the metal (the high point of the Fermi sea) to the semiconductor. These electrons form part of the semiconductor space charge depletion layer (fixed negative charge). This is charge the gate doesn’t have to supply to “turn the MOSFET on.” Thus, the work-function difference lowers the intrinsic threshold by $0.25\, \text{V}$, making $V_{th} = 0.59\, \text{V}$

b. On the grounded source side, the the gate bias minus the channel voltage is $V_g - V_c(y = 0) = 3 - 0 = 3\, \text{V}$. Thus, there is a depletion on the source side. On the drain side: $V_g - V_c(y = L) = 3 - 3 = 0\, \text{V}$. This is well below a turn-on drop and so the drain is pinched off at the drain side and the transistor is operating in saturation.

c. For $V_{gs} = 3\, \text{V}$, the pinch-off potential is: $V_{gs} - V_{th} = 3.0 - 0.6 = 2.4\, \text{V}$. As the drain is at 3 volts also, the potential drop between the channel pinch-off point and the edge of
the drain diffusion is 0.6V. The extent of the uninverted channel from the pinch-off point to the drain is:

$$\Delta L = \sqrt{\frac{2\epsilon_{si}\Delta V_c}{qN_a}}$$  \hspace{1cm} (8)

where $\Delta V_c = 0.6V$. Thus, $\Delta L$ is 0.27$\mu$m. The effective channel length is thus: $2 - 0.27 = 1.73\mu$m.

d. The highest field normal to the semiconductor surface occurs at the source. It is just:

$$E = \frac{V_{gs}}{d_{ox}} = \frac{3}{10^{-6}} = 3MV/cm$$ \hspace{1cm} (9)

This is pretty close to breakdown!

e. The active channel is relatively low resistance, and the drop from the source to the pinch-off point is just 2.4V. We can estimate the field in the undepleted channel by assuming a linear drop across the effective gate length. This gives an inverted channel field (a field pointing opposite the transport direction) equal to $2.4/(1.73 \times 10^{-4}) = 1.4 \times 10^{4}V/cm$. Past the pinch-off point, the field grows parabolically. We can deal with the situation the same way we deal with a normal n+/p junction. The p-depletion is the uninverted channel. We deal with the drain diffusion as though it was a metal slug. The channel depletion finds an “image” in this slug. The charge per unit area in the p-region depletion is:

$$\sigma = qN_a x_{sc} = 1.6 \times 10^{-19} 10^{16} \times 2.7 \times 10^{-5} = 4.3 \times 10^{-8}$$ \hspace{1cm} (10)

Of course, the maximum electric field occurs right at the metallurgical junction (in this case, right at the edge of the drain slug):

$$E_{max} = \frac{\sigma}{\epsilon_{si}} = 4.3 \times 10^{4}V/cm$$ \hspace{1cm} (11)

Even for this “long-channel” device, the maximum drain field is over three times that of the inverted channel. This is known as the high field drain.

3. A major circuit affected by body effect is the source follower. Clearly, if the substrate is grounded, the output node (the source) can’t be grounded too. In that case, the output would be clamped to zero. So, as the source-to-drain current increases, the source node becomes more positive. This increases the reverse body bias, which raises the threshold. This, in turn lowers the drain current. Thus, what is ostensibly a highly linear circuit develops harmonic distortion.

**DIODES**

1. Consider the following circuit:

   We start with the diode in deep reverse bias. No current flows. This implies no drop across the resistor, R. $V_o =$ is therefore -5V. Now we switch the terminal bias rapidly to
+5V - forward biasing the diode. \( V_o \) raises rapidly to 0.7 volts - the built in voltage of the junction. There is some RC - rounding to the rise due to the 1K resistor and the sum of the space charge and diffusion capacitances. Note: as we discussed in class, the space charge in forward bias never really shrinks to zero. Before that happens, the parasitic resistances “gobble up” (note the Thanksgiving metaphor) the extra potential drop and the drop across the junction freezes. The “rule of thumb” is that the junction shrinks to half its equilibrium thickness. And so:

\[
x_{sc} = \frac{1}{2} \sqrt{\frac{2\varepsilon_{si}V_{bi}}{qN_a}} \tag{12}
\]

and:

\[
C_{sc} = \frac{\varepsilon_{si}}{x_{sc}} \tag{13}
\]

The diffusion capacitance is fairly easy to compute. It’s just:

\[
C_{diff} = \frac{I_d \tau}{V_{thermal}} \tag{14}
\]

Here, the diode current is just:

\[
I_d = \frac{5 - .7}{1000} \tag{15}
\]
where $V_{thermal}$ is the thermal voltage, 0.0259V. The total capacitance, $C_{tot}$ is $C_{sc} + C_{diff}$.

And the rise-time constant is $RC = R(C_{sc} + C_{diff})$.

Making the transition from forward to reverse bias, though is a whole different matter. The diode stays in forward bias ($V_0 = 0.7$) until all the minority charge can recombine. This is called the storage lifetime. As we derived in class, the storage lifetime is:

$$\tau_{stor} = \tau_{minority} Ln \left[ \frac{(i_f - i_r)}{-i_r} \right]$$  \hspace{1cm} (16)

where $i_f$ and $i_r$ are the same here:

$$I = \frac{(5 - 0.7)}{1000}$$  \hspace{1cm} (17)

After a storage lifetime, the diode returns to it’s equilibrium reverse situation and $V_0$ returns to -5 V. But before it does this, there is still an added RC delay. Here, though, the diode is reverse biased and there is no diffusion capacitance to account for. The $C$ in the RC is just $C_{sc}$ as given above.

PLEASE CHECK THE WEBSITE TOMORROW! I’LL TRY TO ADD SOME MORE "INFORMATIVE" ILLUSTRATIONS.