

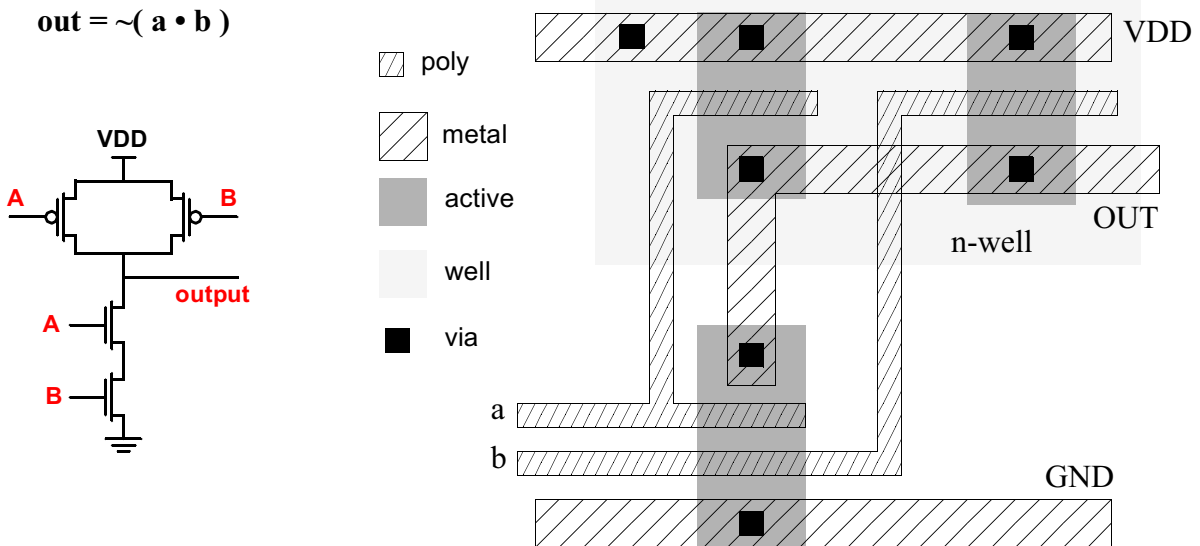
# Homework 2

ENEE 359a: Digital VLSI Design

Assigned: Tue, Mar 4 Due: Tue, Mar 11

## 1. Logic to Circuit to Layout

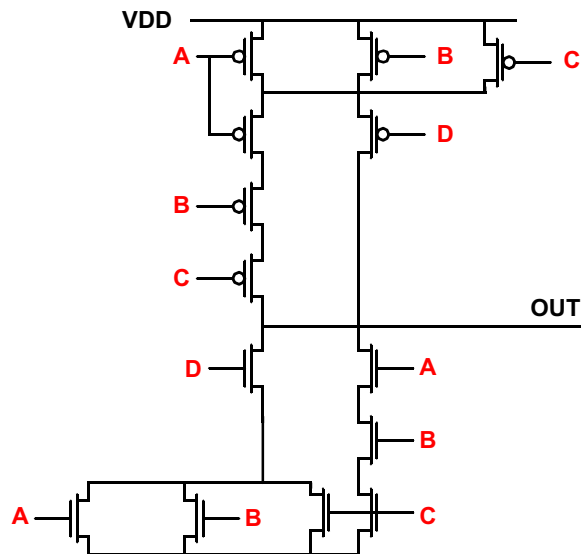
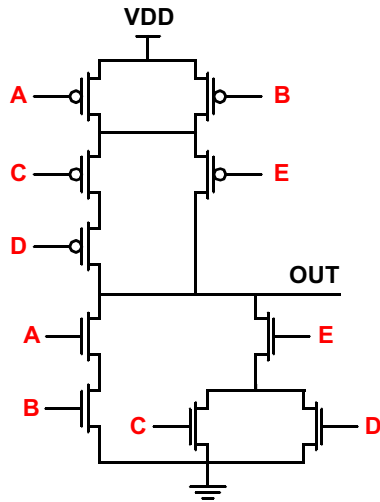
Convert the following logical expressions to schematic diagrams for static CMOS logic. Then convert each to a rough layout assuming an n-well process (e.g. p-type wafer: nFETs can be built directly on the wafer); you need only show wells for pFETs. The following is an example:



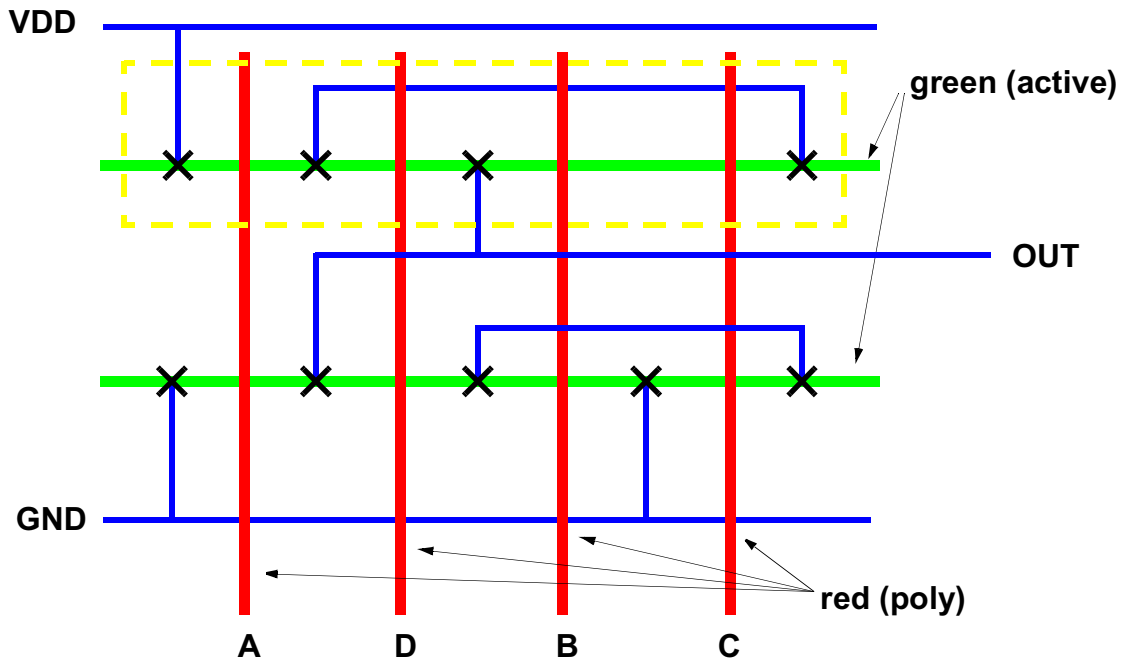
- A.  $out = \sim((a \cdot b) | c)$
- B.  $out = \sim((a | b) \cdot c)$
- C.  $out = \sim(a \cdot b \cdot (c | d))$
- D.  $out = (a + b)$ ;  $c_{out} = (a + b = 10_2)$  (carry-out only; no carry-in)  
 [do the full circuit diagram, but do not spend more than 20 minutes trying to do the layout for this; it is not simple AOI logic ... make enough of an attempt to understand the difficulty of dealing with inverted values]

## 2. Layout to Circuit to Logic

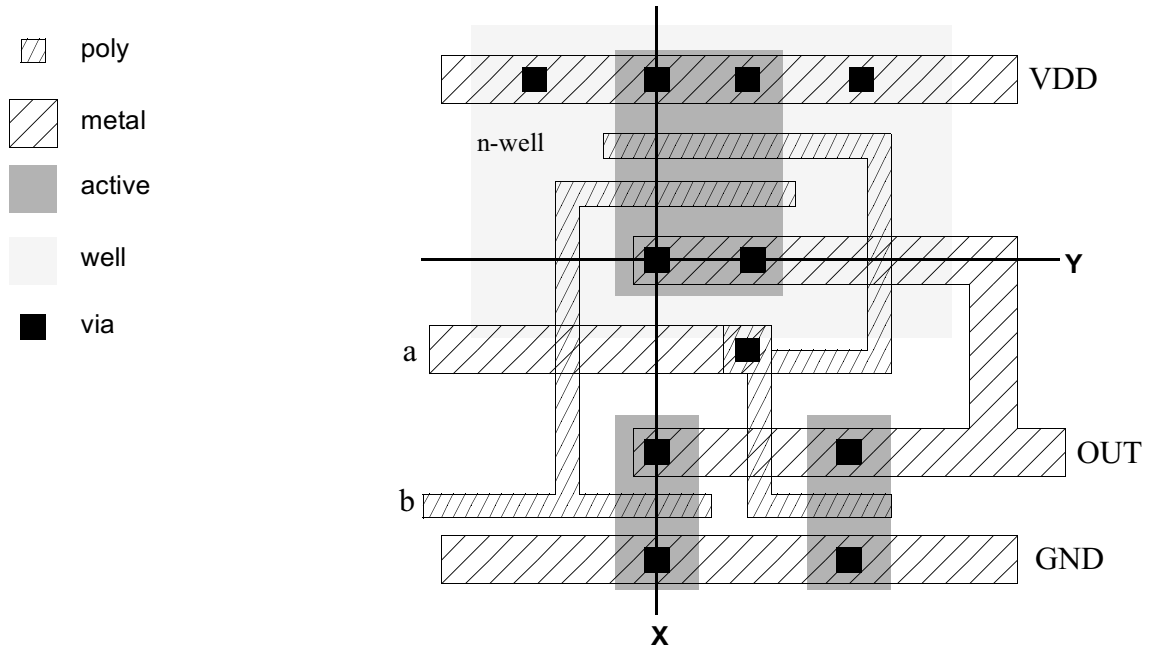
A. What logic equations do the following schematics implement?



B. Consider the following stick diagram. Draw the transistor-level schematic. What logic equation does the circuit implement?



C. Provide a side-view diagram for each of the cuts X and Y through the layout below. Be sure to label each of the strata.



D. What is the logic equation represented by the layout in question C?