ENEE 359a *Digital VLSI Design*

Sequential Logic

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Credit where credit is due:
Slides contain original artwork (© Jacob 2004) as well as material taken liberally from Irwin & Vijay's CSE477 slides (PSU), Schmit & Strojwas's 18-322 slides (CMU), Dally's EE273 slides (Stanford), Wolf's slides for *Modern VLSI Design*, and/or Rabaey's slides (UCB).

Overview

- Transmission gates
- Basic storage-cell concepts
- Metastability
- Static latches & registers, brief primer on dynamic logic, dynamic latches & registers, trading off complexity in individual memory elements vs. complexity in clock-delivery network
- Pipelining

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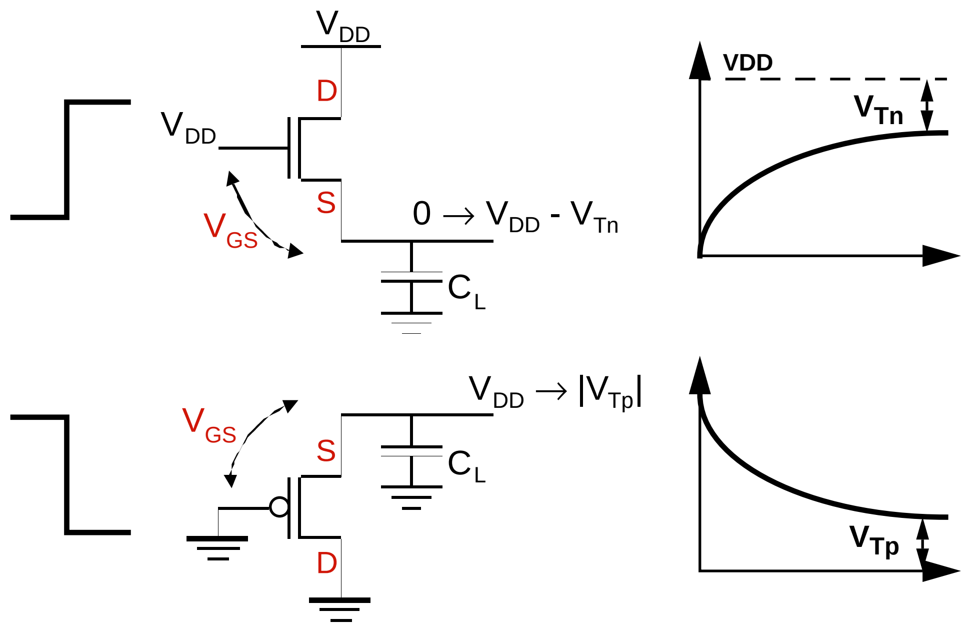
The Transmission Gate

Basic idea: reduce number of transistors in design by allowing inputs to drive not only *gate* terminals but also *source/drain* terminals.

(similar in this regard to *pass-transistor* logic)

Recall:

- **NMOS will not pass a “1”**
- **PMOS will not pass a “0”**



- **Body effect ($V_{BS} \neq 0$) causes $V_{Tn/p}$ to increase**

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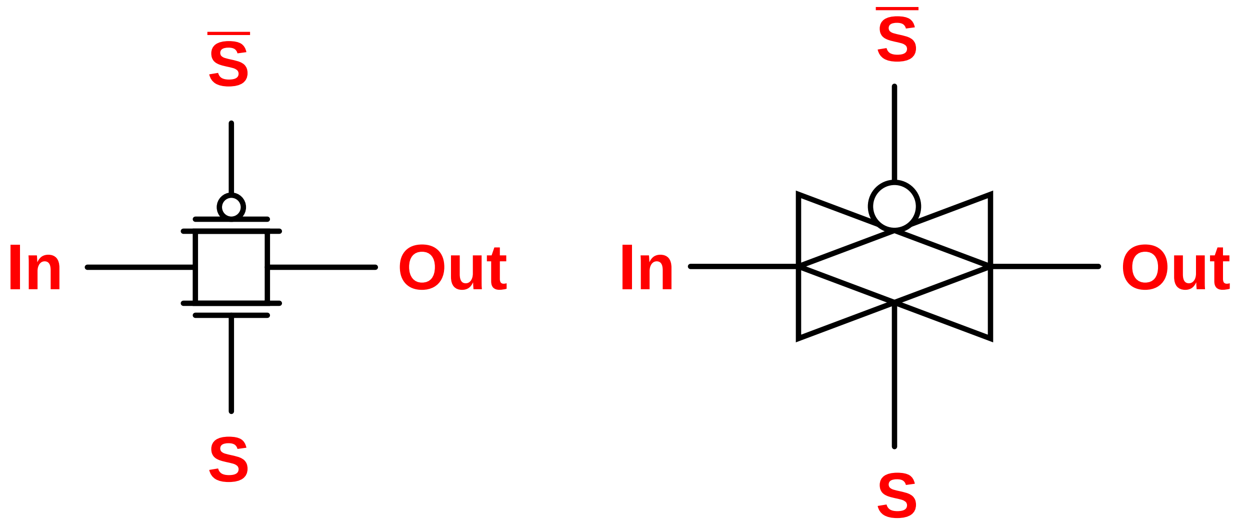
Solution: use both



Out = (S) ? In : Z;

Potential problem: unlike other static logic gates, this can allow output to be *floating* (not connected — thus, easily perturbed by nearby signals such as metal wires above)

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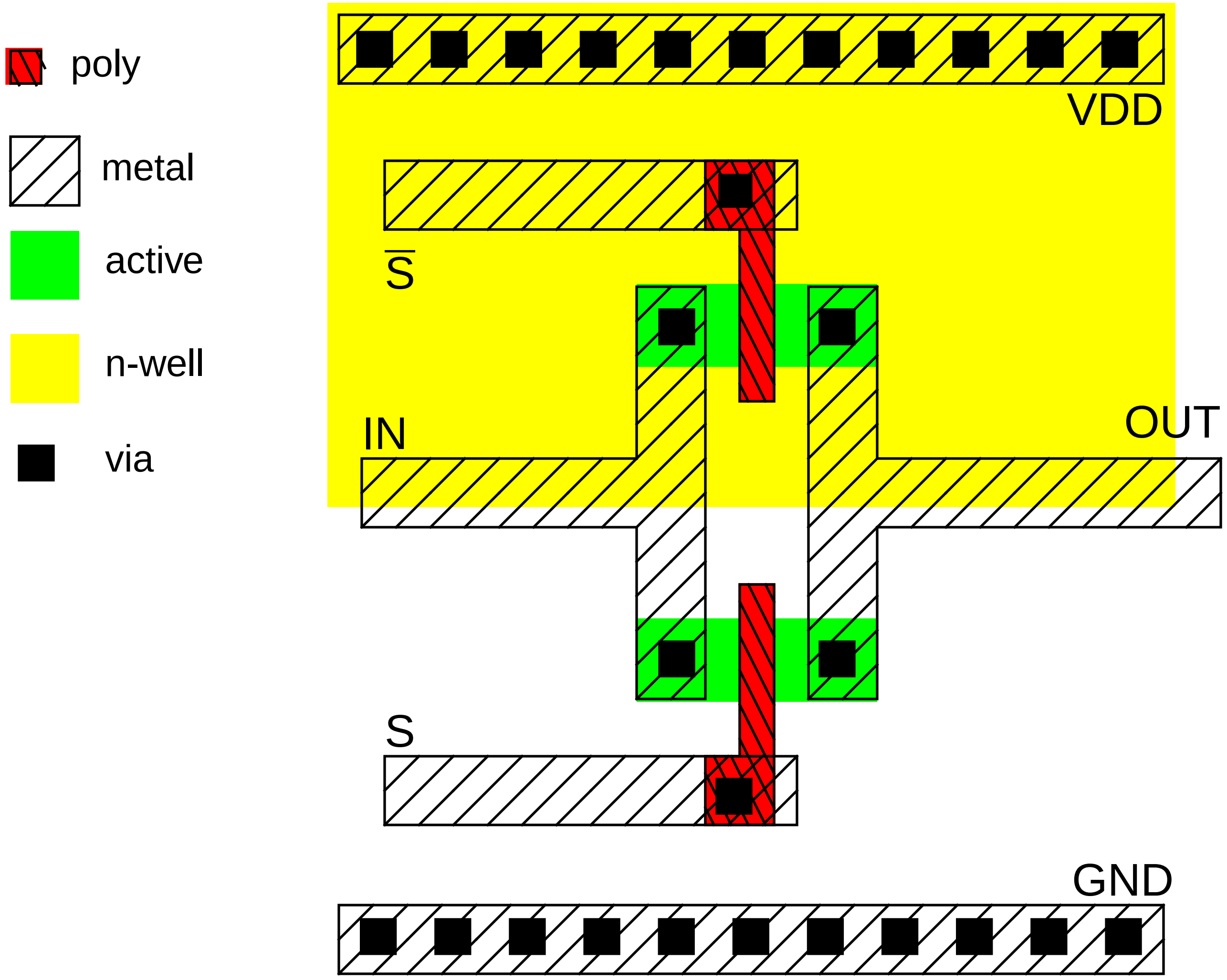
The Transmission Gate



Sometimes standard cell includes S inverter

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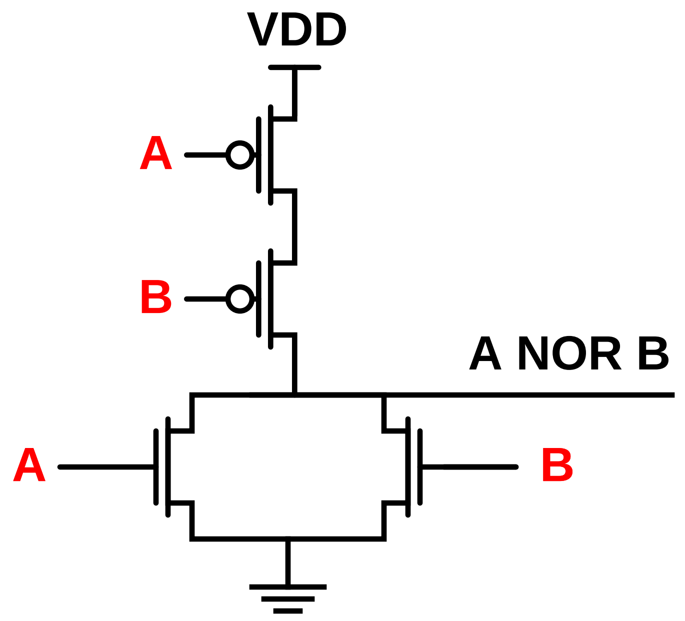
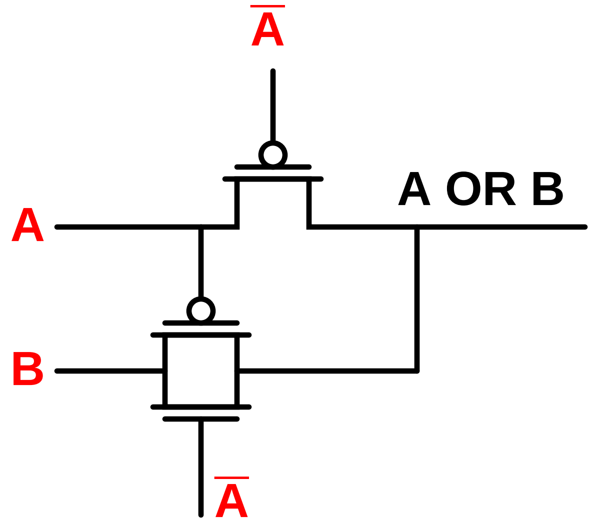
The Transmission Gate



Complementary Implementation

TG Implementation



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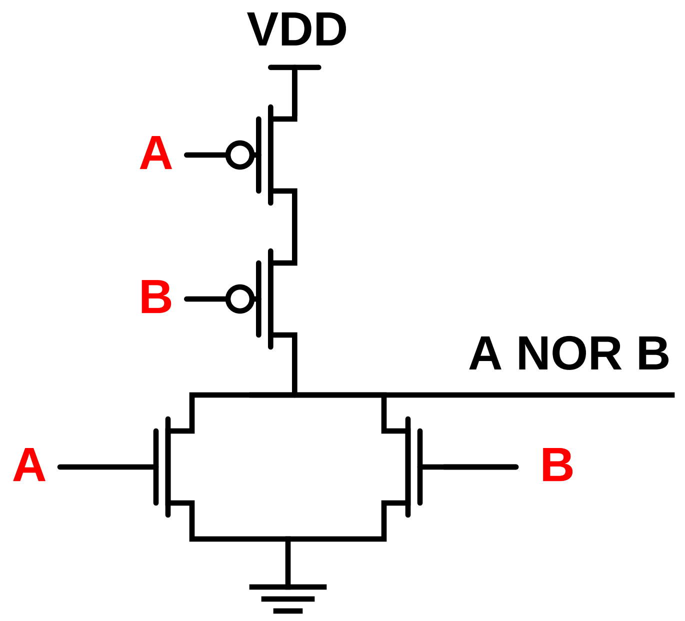

Complementary
Implementation

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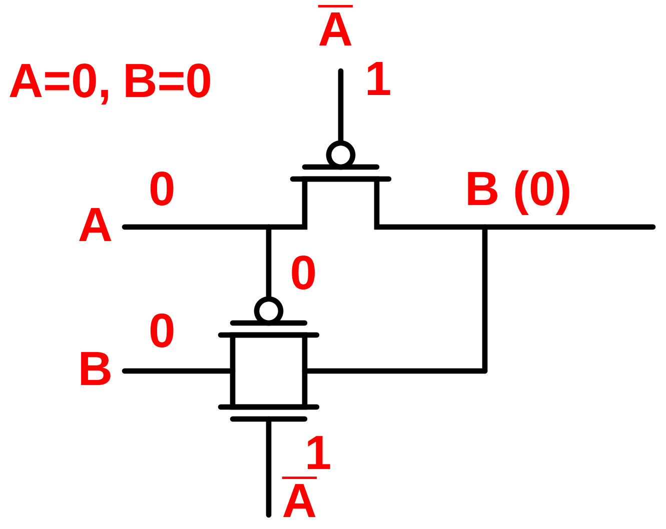

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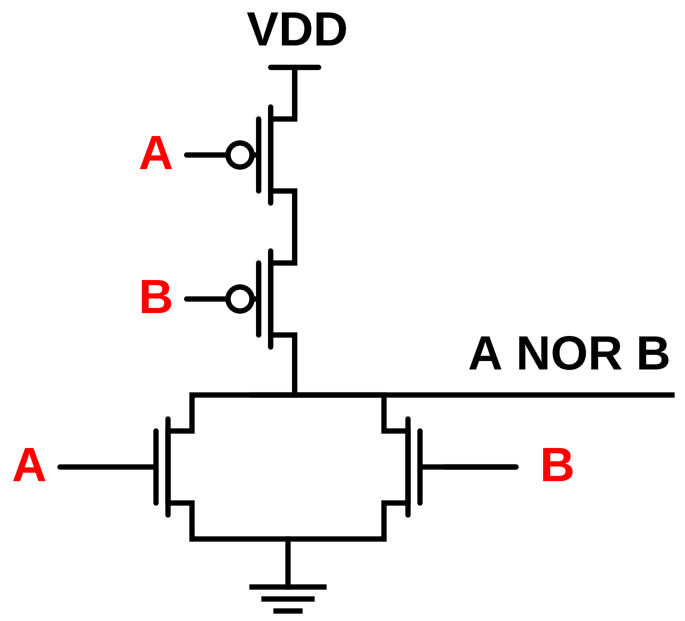

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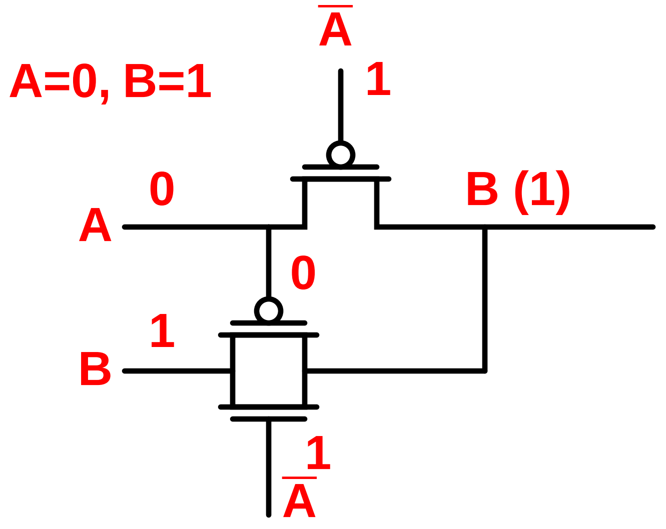

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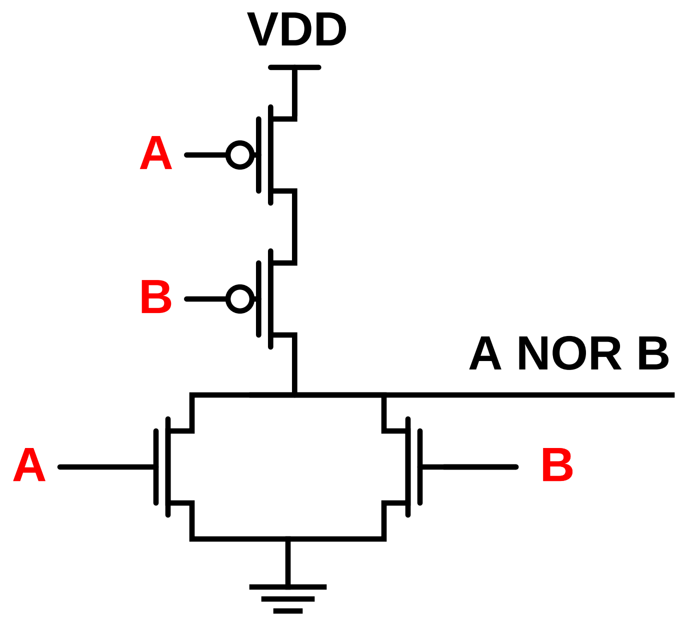

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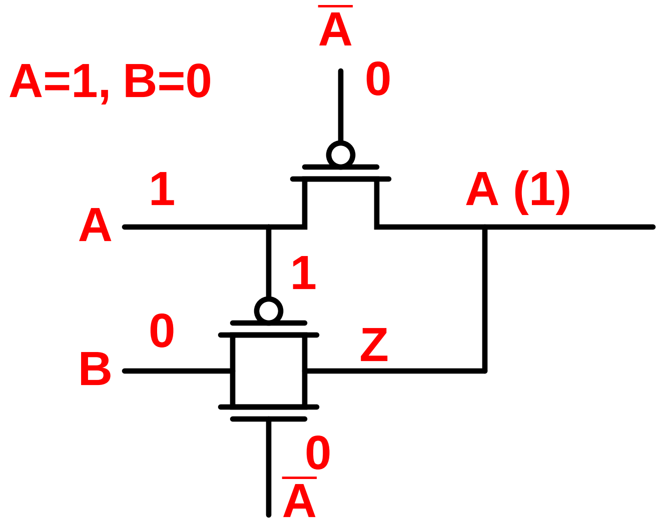

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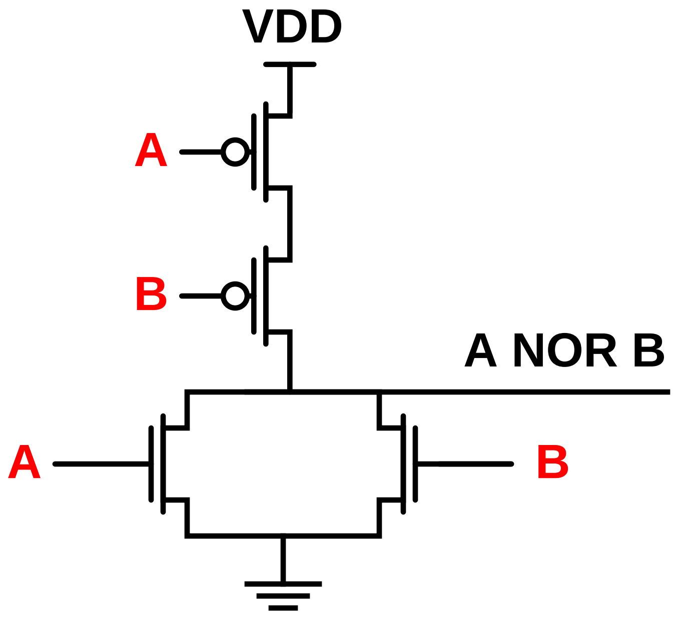

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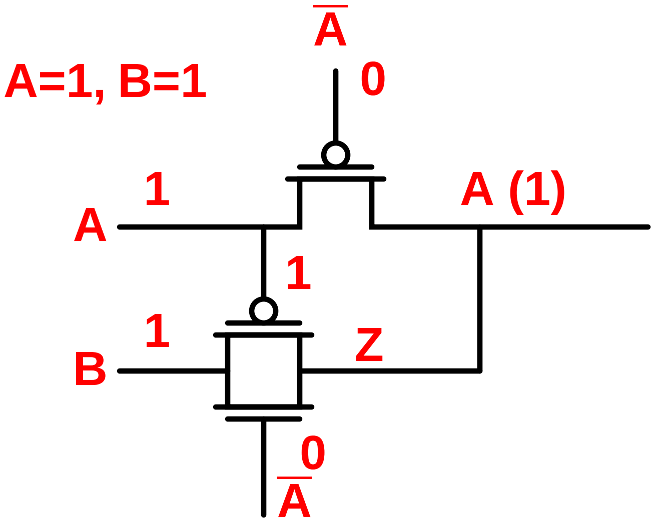

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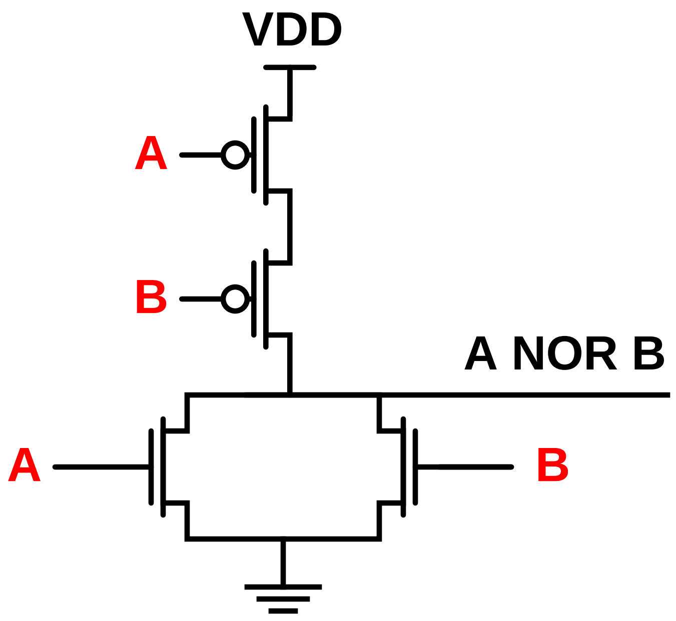
The Transmission Gate



Complementary Implementation

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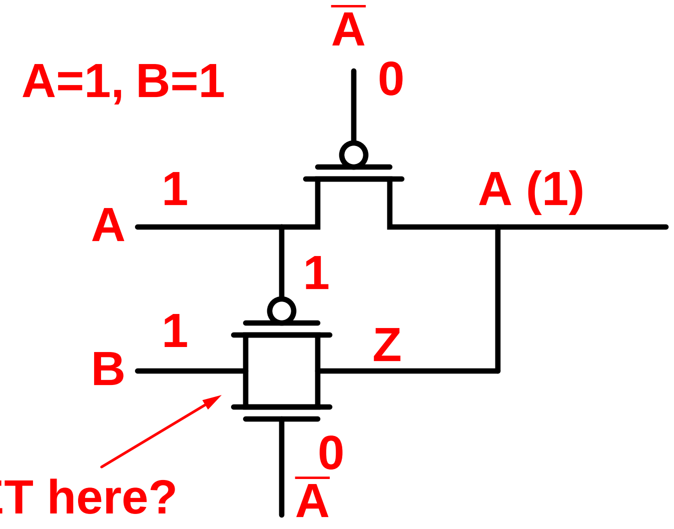

Q: why can't we just use nFET here?

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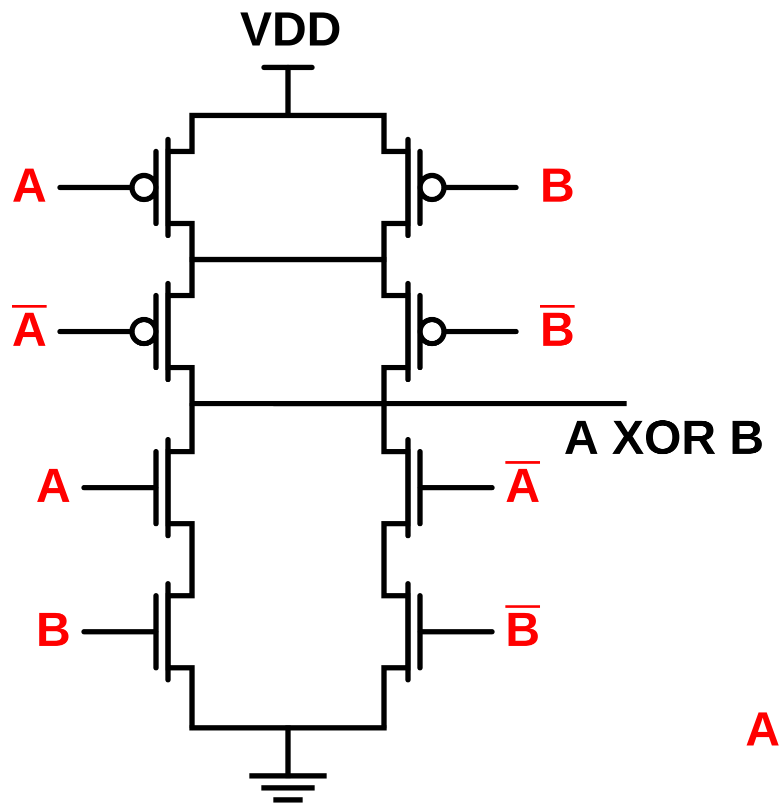

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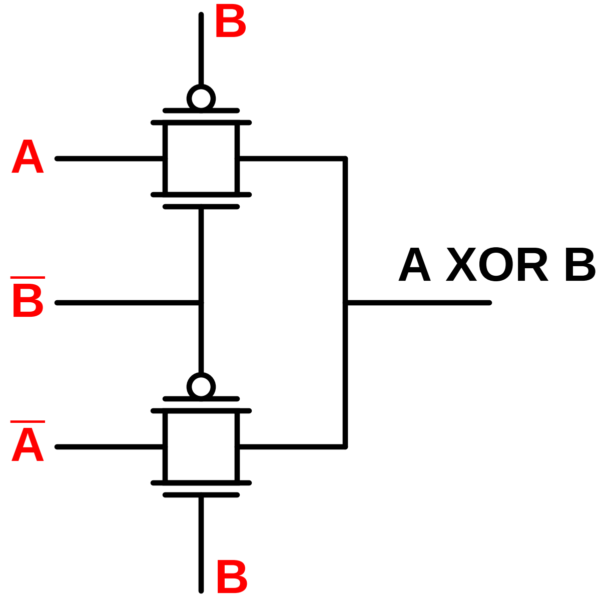

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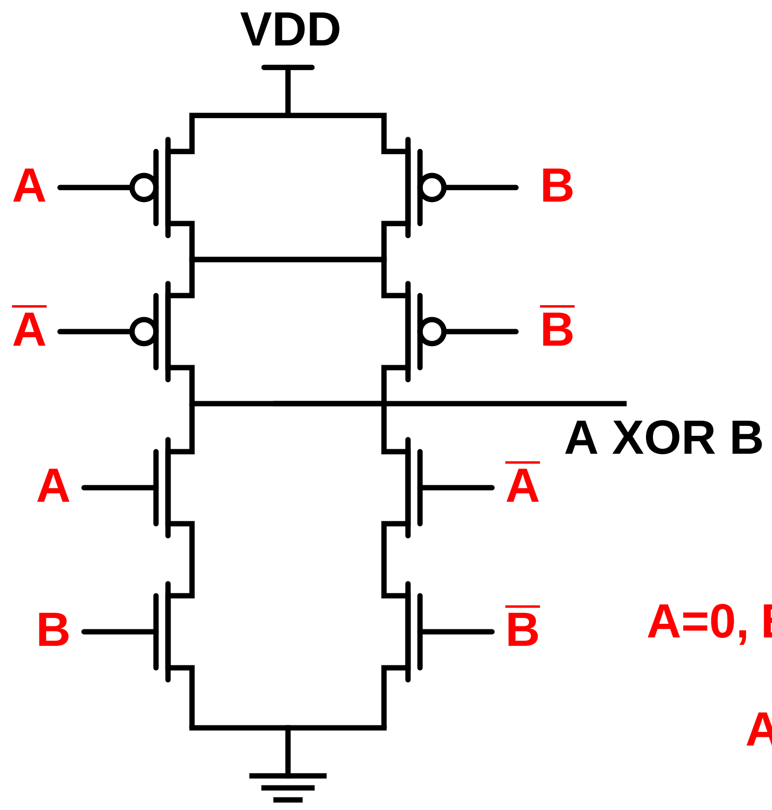

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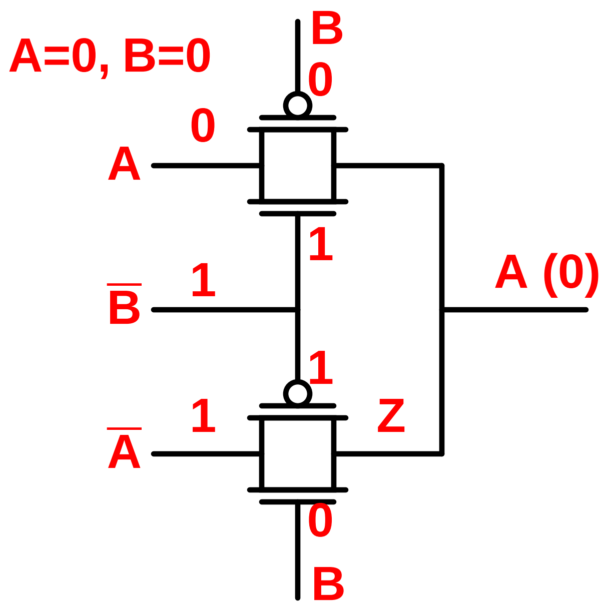

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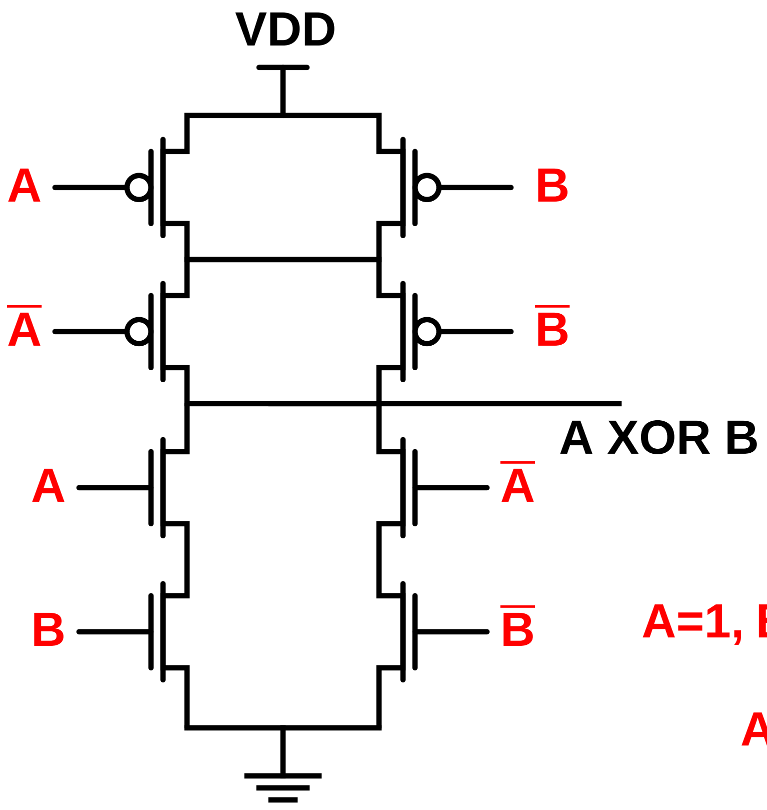

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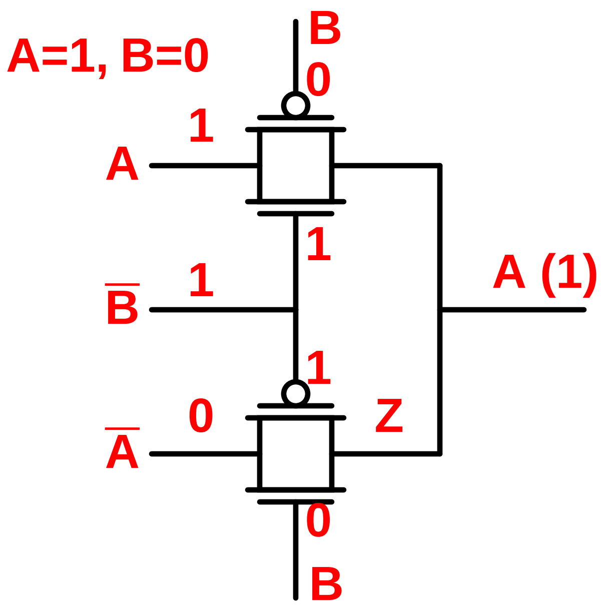

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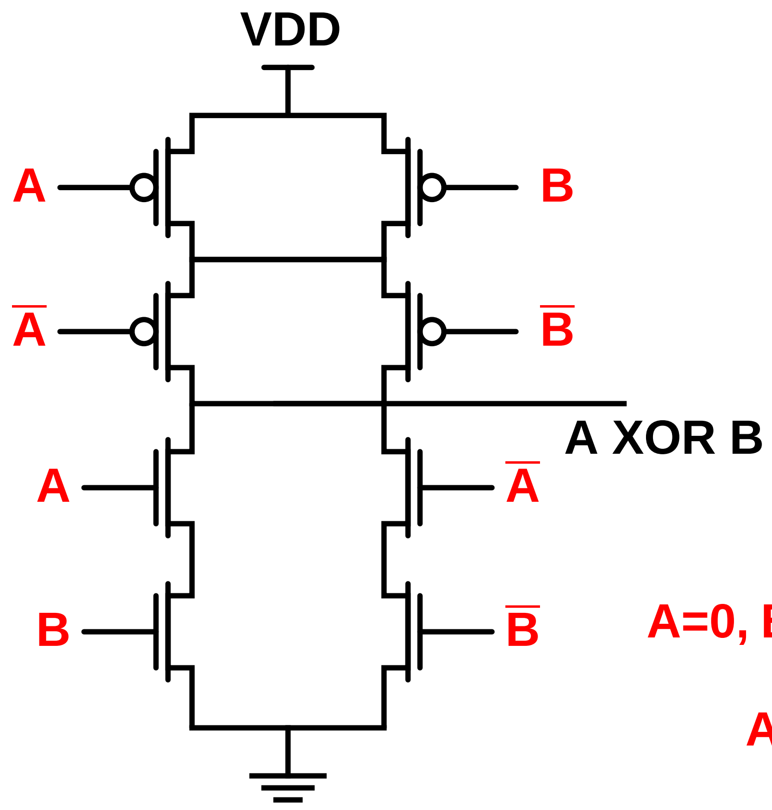

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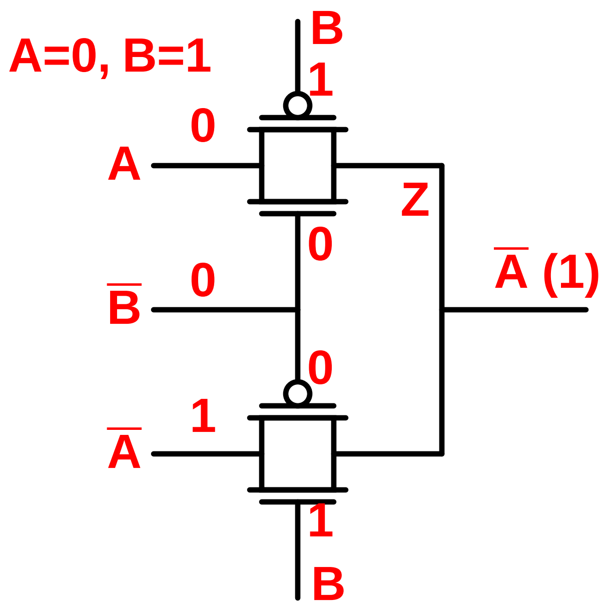

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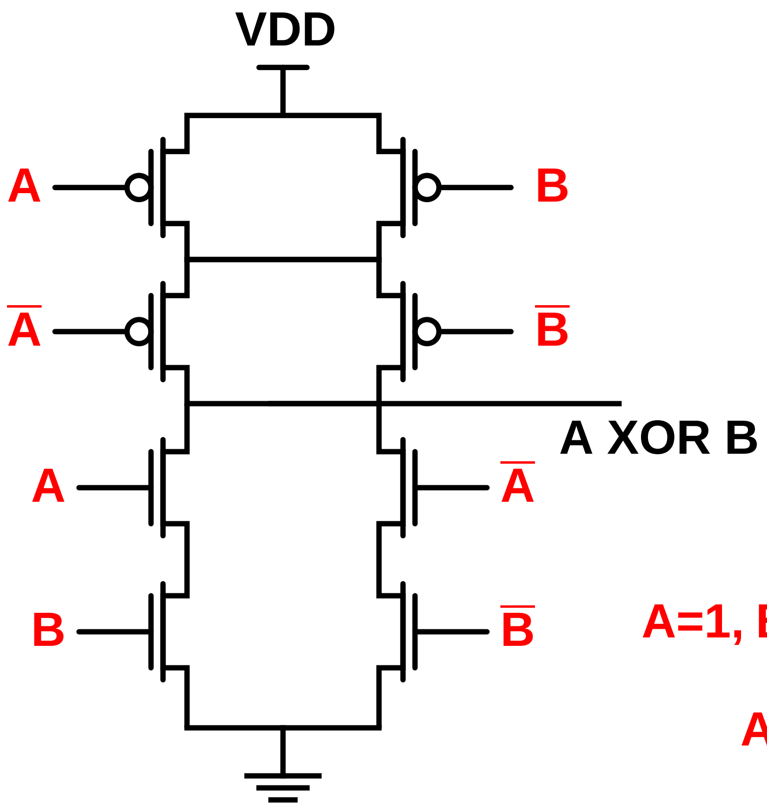
The Transmission Gate



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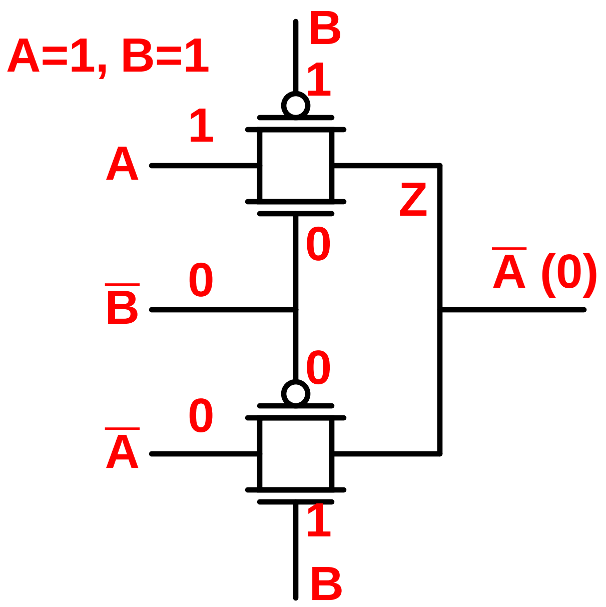

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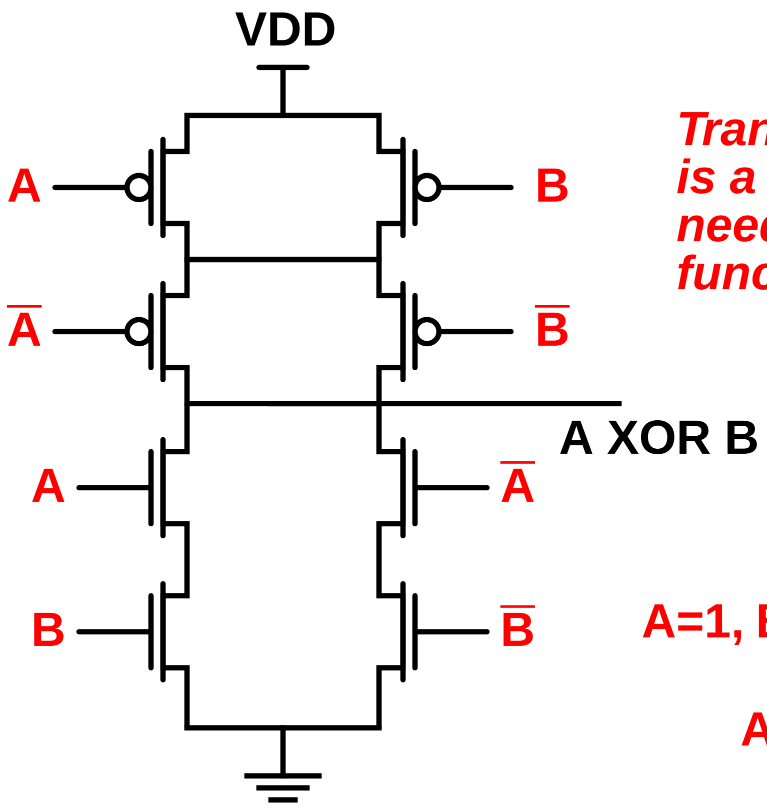
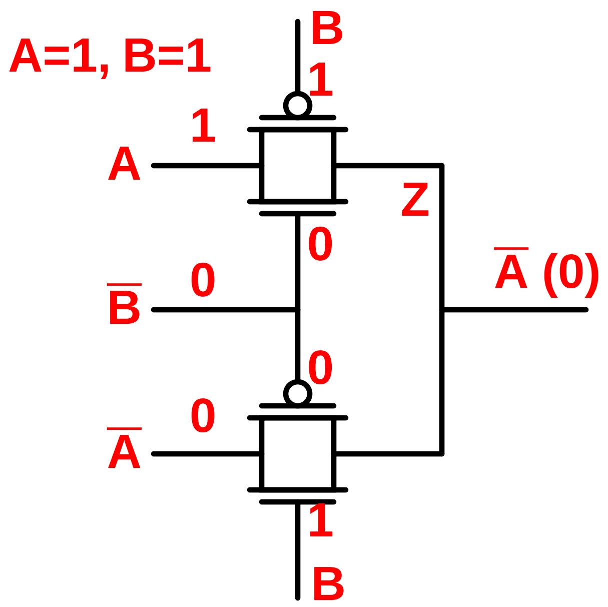


Complementary Implementation

Transmission-gate logic is a huge win for circuits that need XOR/XNOR and similar functions, e.g. full adders

XOR = A$\overline{B}$ + $\overline{A}$B

TG Implementation



Basic storage-cell concepts

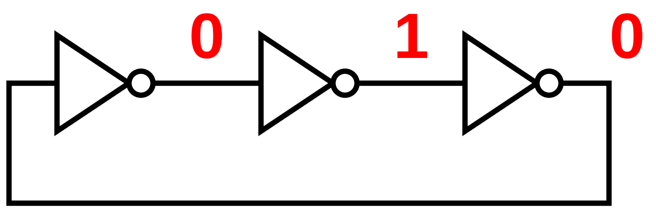
DEFINITIONS (from the book):

1. **Flip-flop: bistable component built by cross-coupling logic gates**
2. **Latch: *level-sensistive* storage element**
3. **Register: *edge-triggered* storage element**

**(the literature on the topic is not consistent in its use of these terms,
so beware and try to figure out from context what someone means …)**

Basic storage-cell concepts

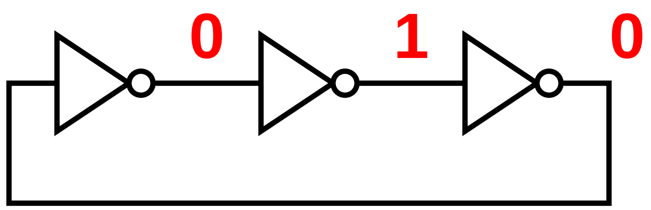
Bistable? Only two stable points on VTC



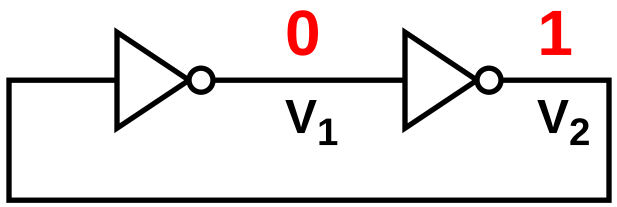
… what happens next?

Basic storage-cell concepts

Bistable? Only two stable points on VTC



… what happens next?



… what happens next?

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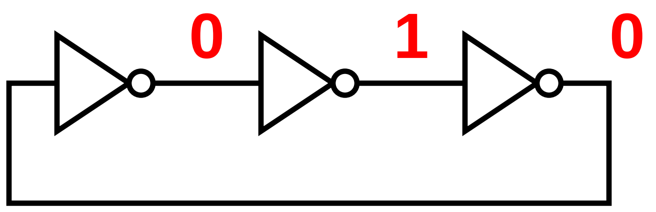
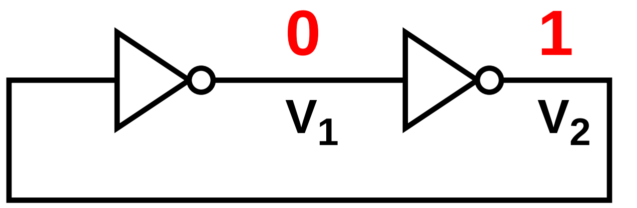
Basic storage-cell concepts

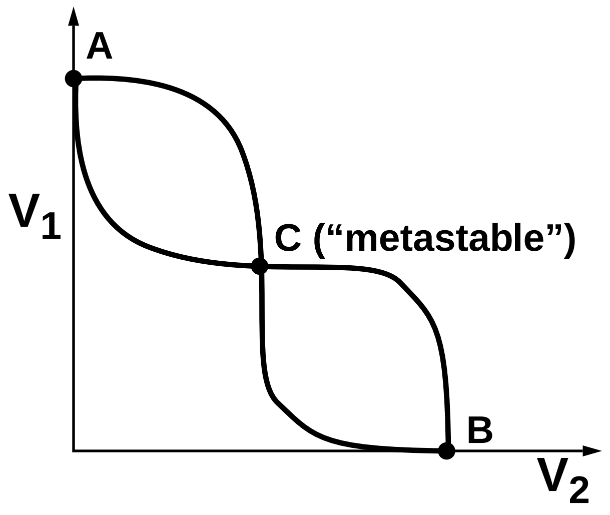
Bistable? Only two stable points on VTC



… what happens next?



this is a stable circuit
(and, in particular, bistable)



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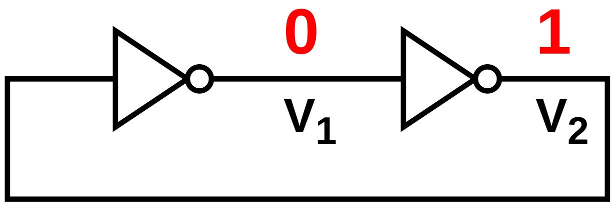
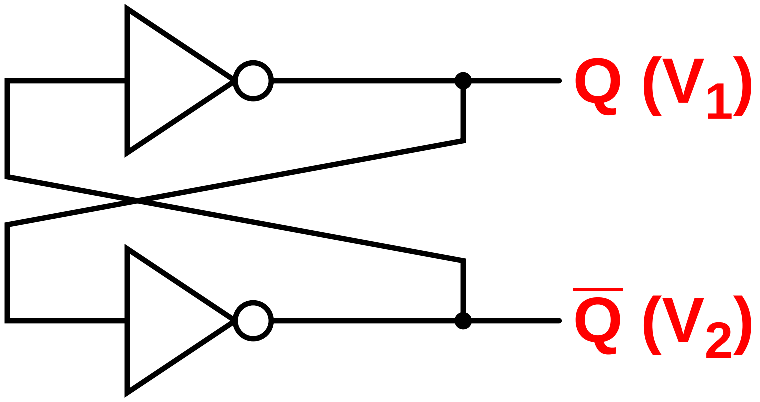
Basic storage-cell concepts

Cross-coupling? Memory as feedback

This:



Equals this:



Question: how do we write a new value?

- Cutting feedback loop (multiplexer-based)
- Overpowering feedback loop

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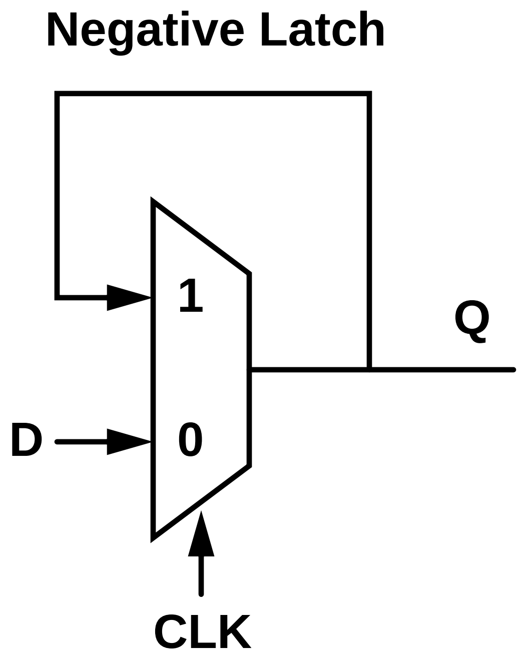
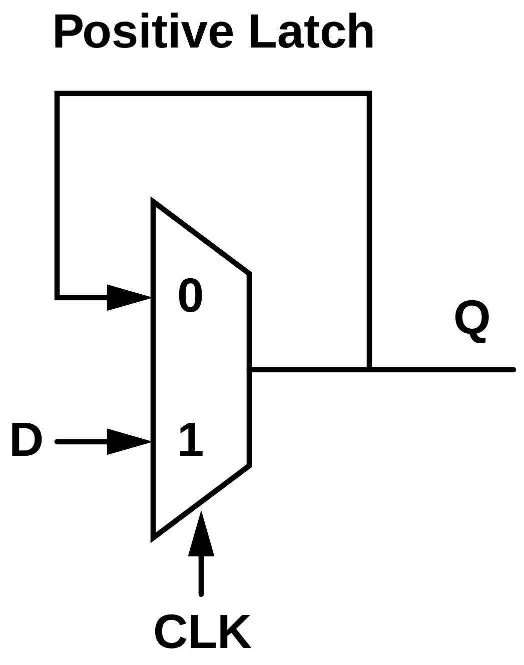
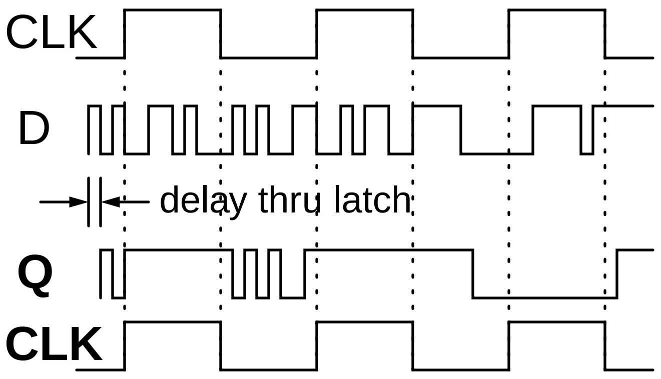
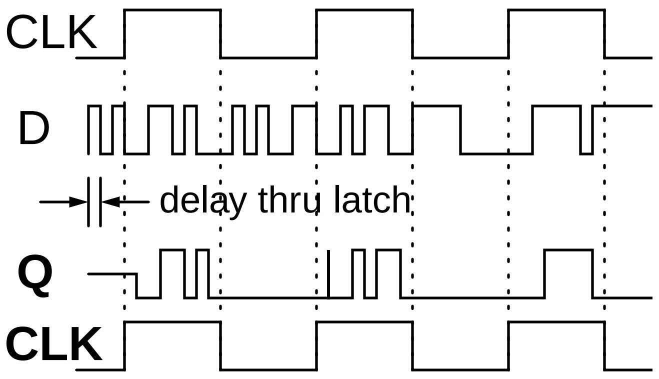
Multiplexer-Based Latches









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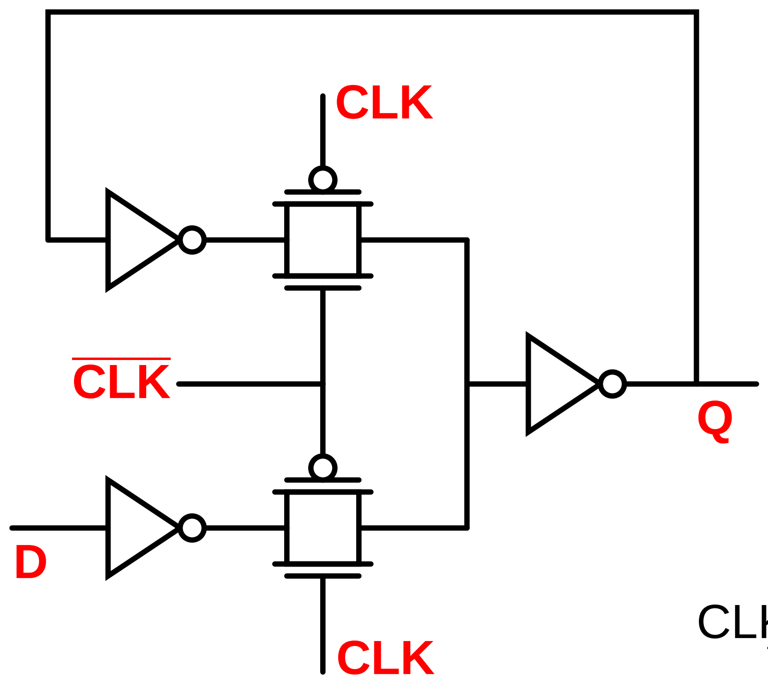
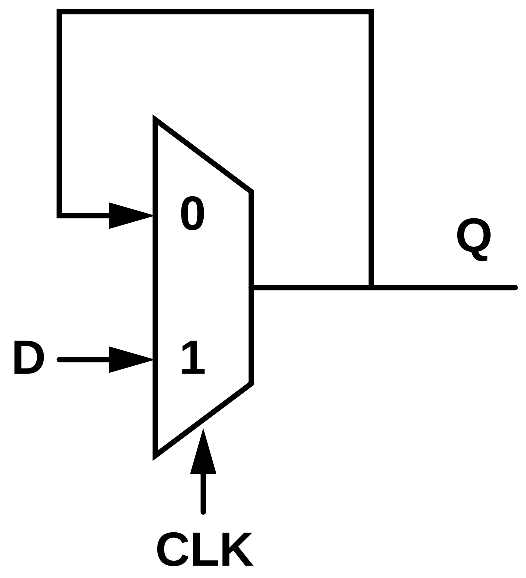
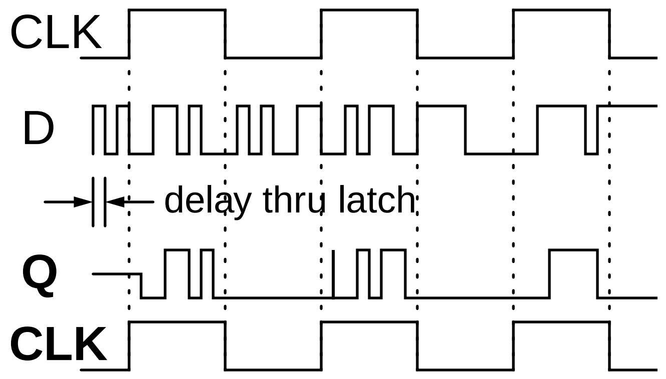
Multiplexer-Based Latches



Positive Latch





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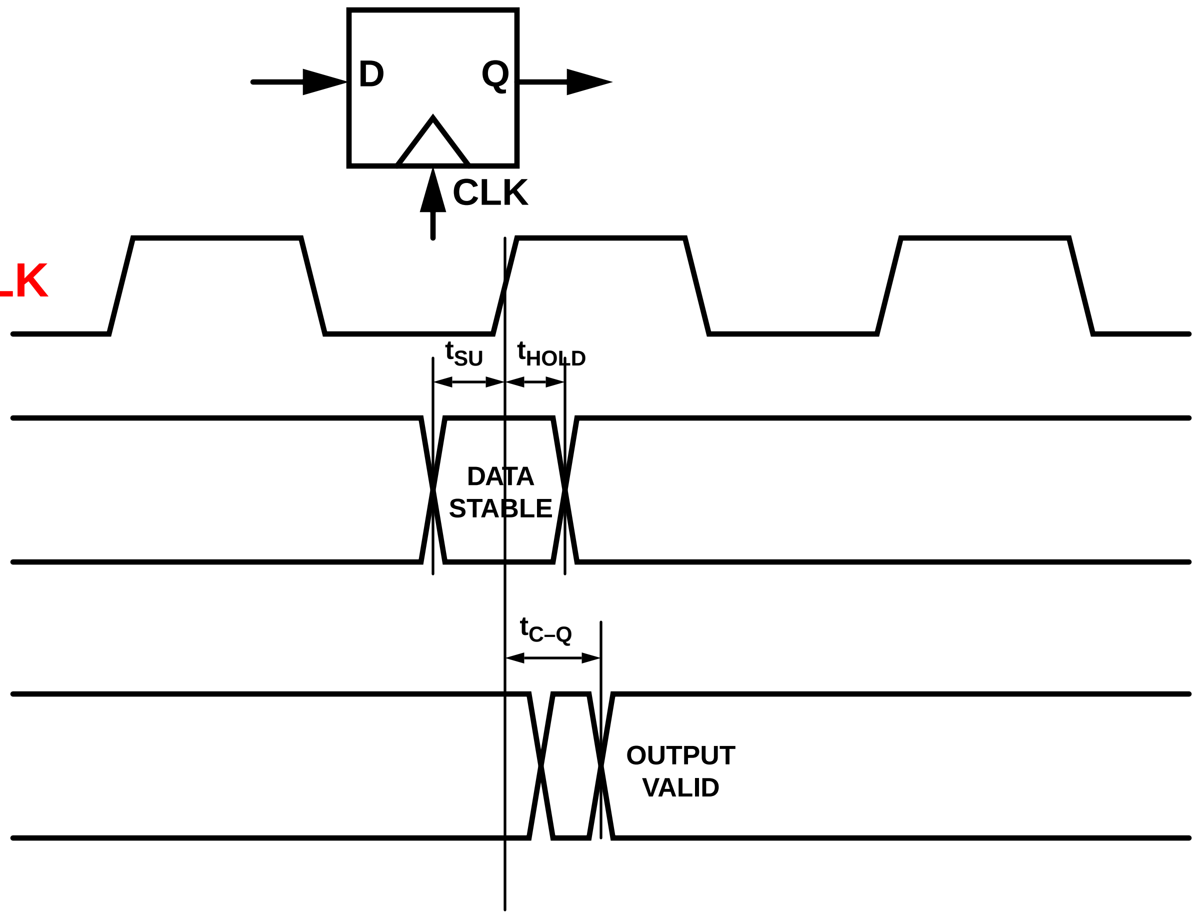
Metastability

SET-UP and HOLD times



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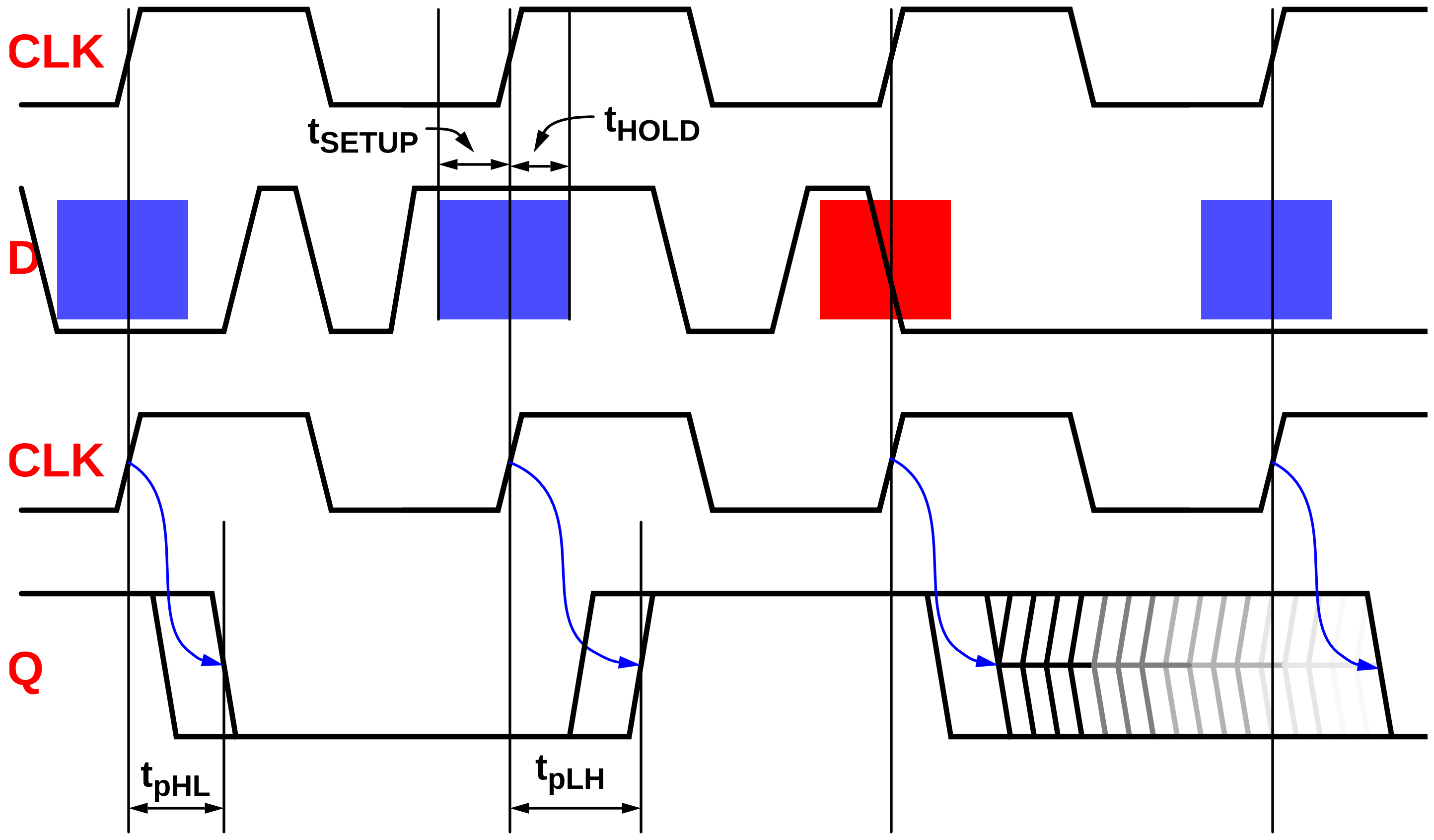
Metastability

SET-UP and HOLD time violations



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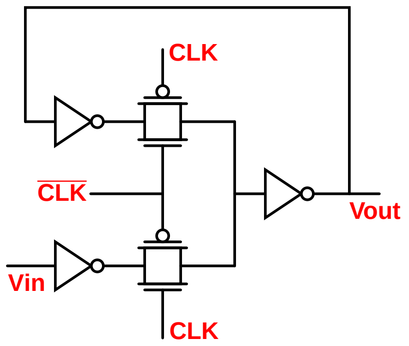
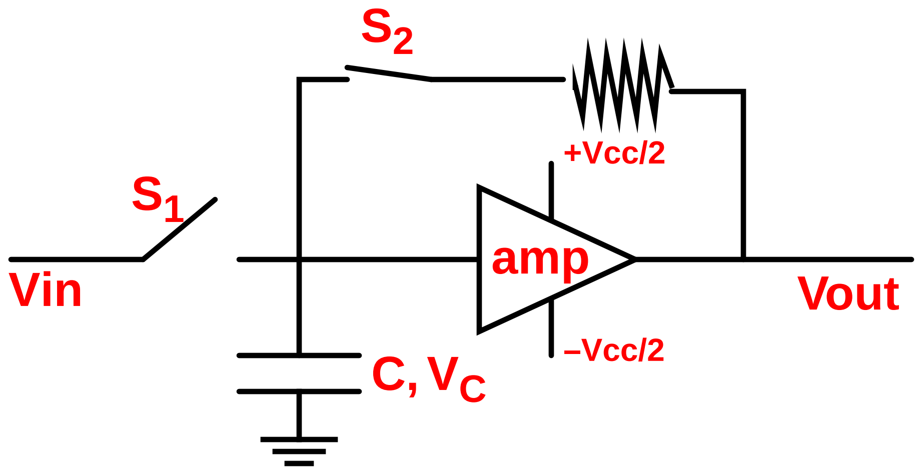
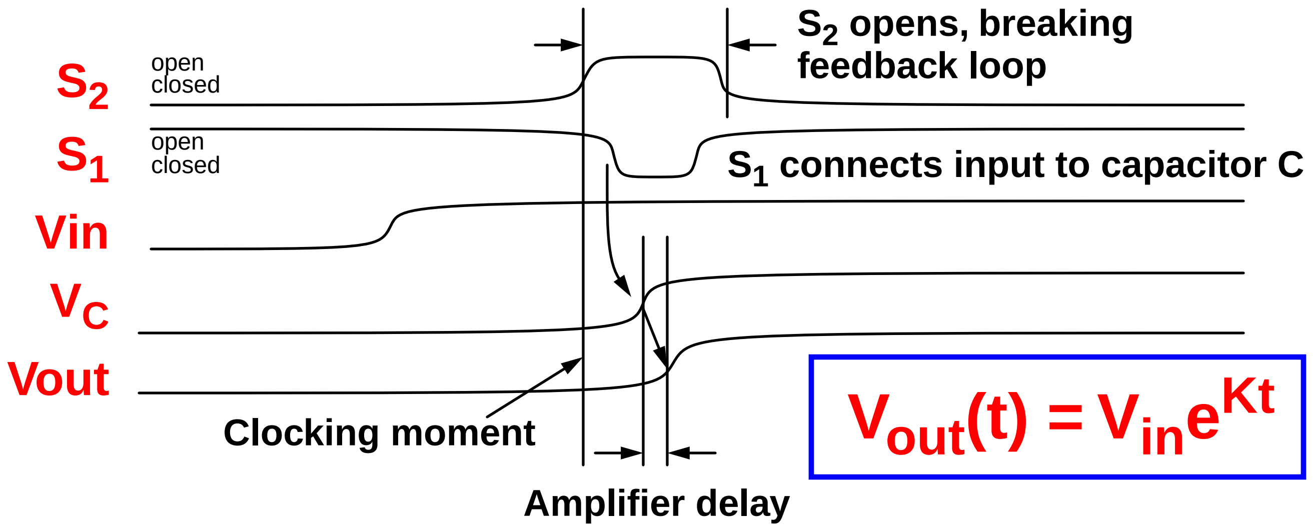
Metastability

Intuition behind the behavior







$$\boxed{V_{out}(t) = V_{in}e^{Kt}}$$

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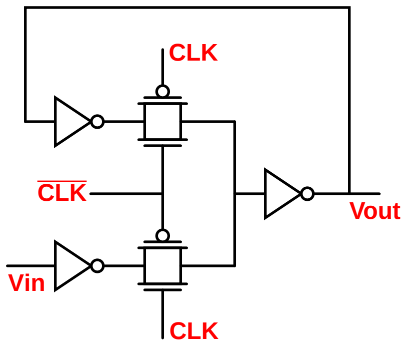
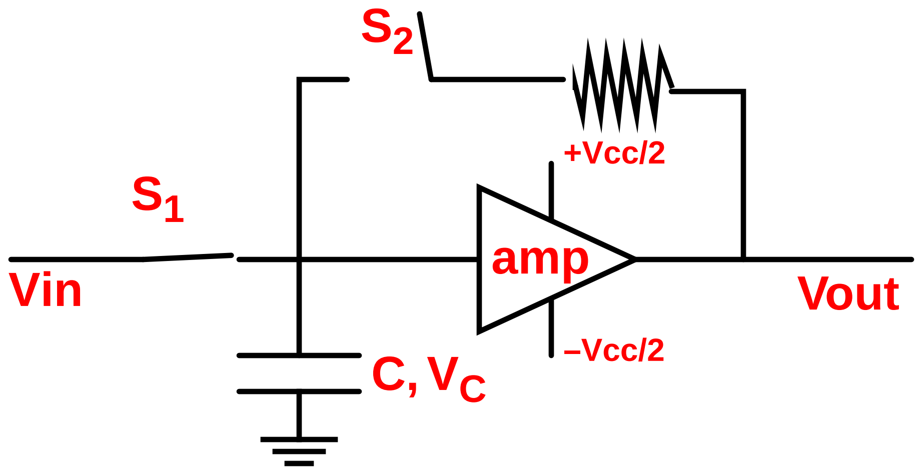
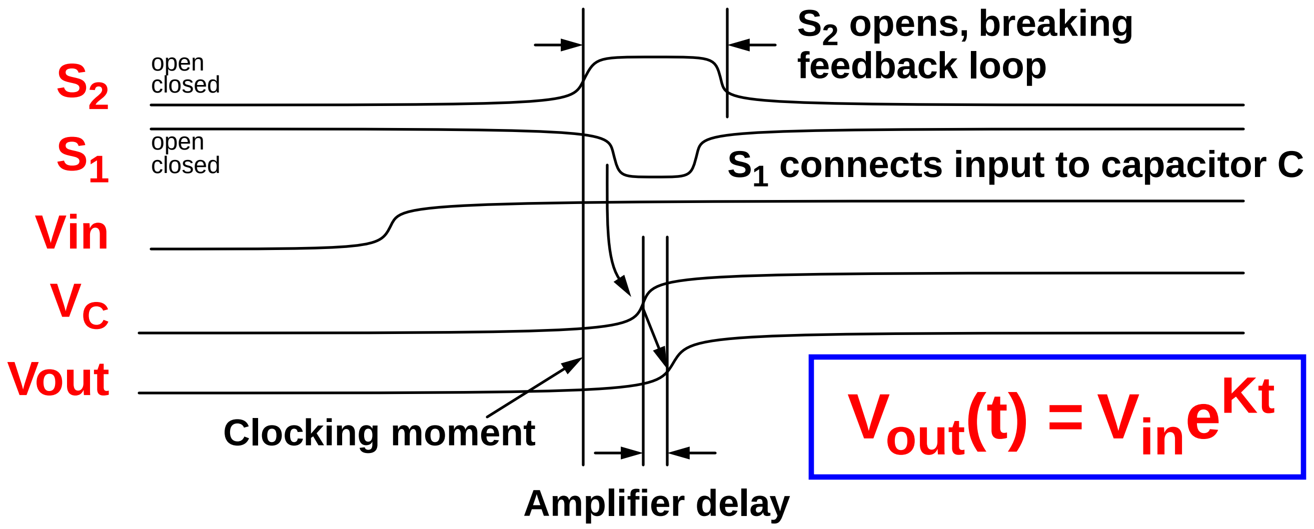
Metastability

Intuition behind the behavior



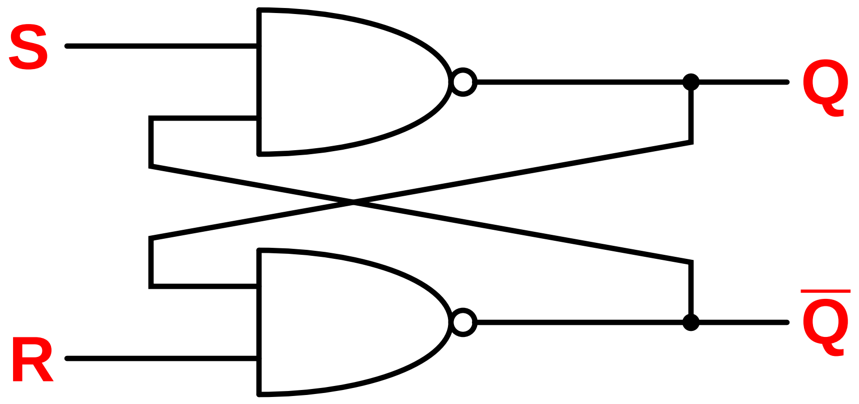




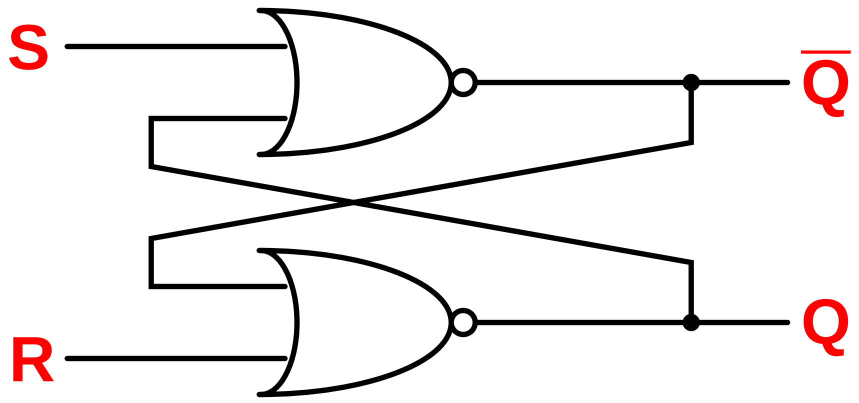
$$\boxed{V_{out}(t) = V_{in}e^{Kt}}$$

Static latches & registers

Set-Reset Flip-Flop (two types)



S	R	Q	$\overline{Q}$
0	0	1	1
1	0	0	1
0	1	1	0
1	1	Q	$\overline{Q}$



S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

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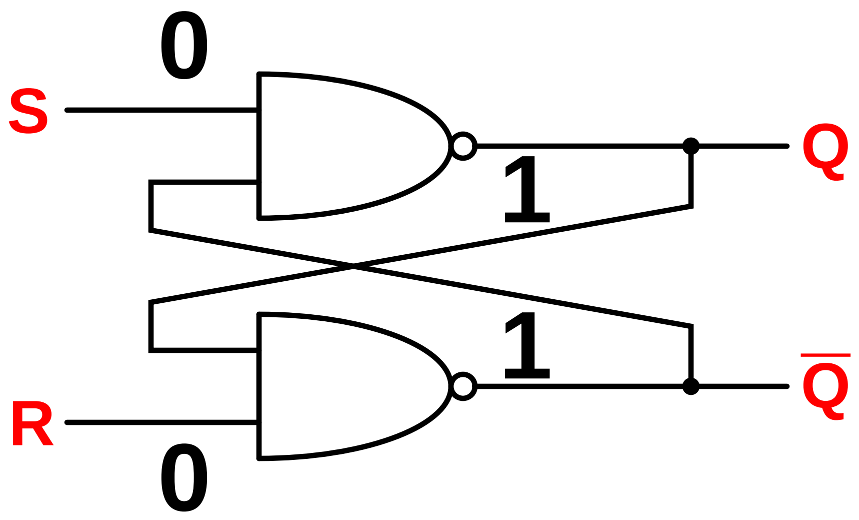
Static latches & registers

NAND-based SR Flip-Flop

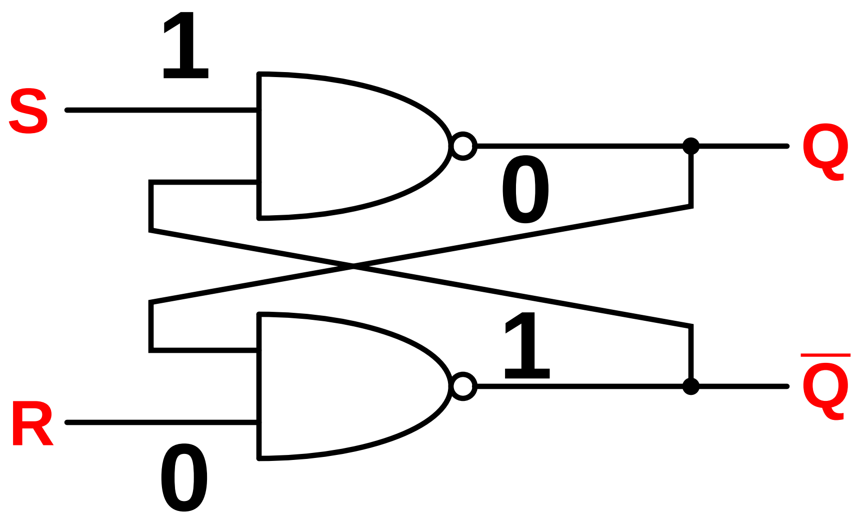


S	R	Q	$\overline{Q}$
0	0	1	1
1	0	0	1
0	1	1	0
1	1	Q	$\overline{Q}$

“forbidden” state, Q == $\overline{Q}$

Static latches & registers

NAND-based SR Flip-Flop



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1	0	0	1
0	1	1	0
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Static latches & registers

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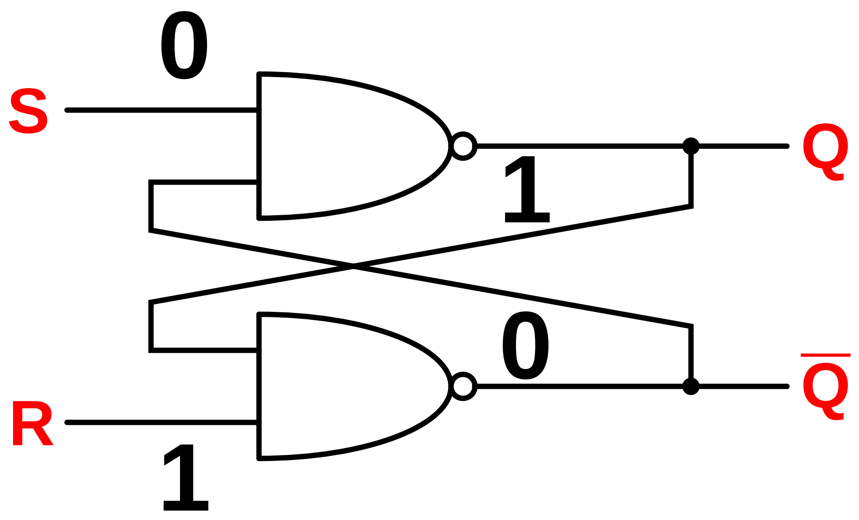
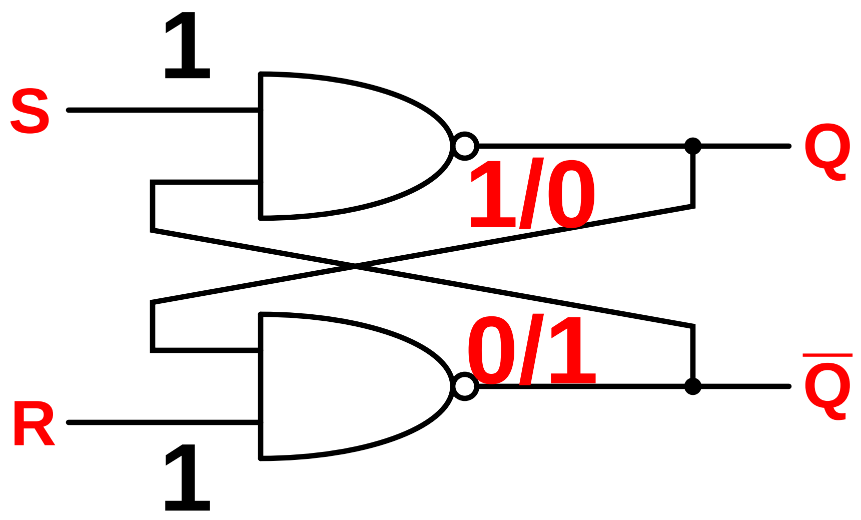


S	R	Q	$\overline{Q}$
0	0	1	1
1	0	0	1
0	1	1	0
1	1	Q	$\overline{Q}$

Static latches & registers

NAND-based SR Flip-Flop

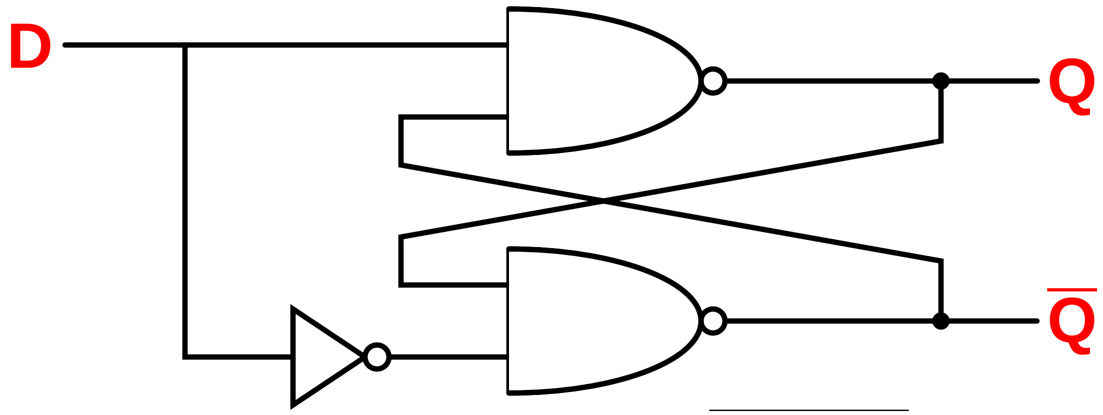


S	R	Q	$\overline{Q}$
0	0	1	1
1	0	0	1
0	1	1	0
1	1	Q	$\overline{Q}$

Q and $\overline{Q}$ keep their previous values if this state is reached from a non-forbidden state

Some Issues

Forbidden FF states

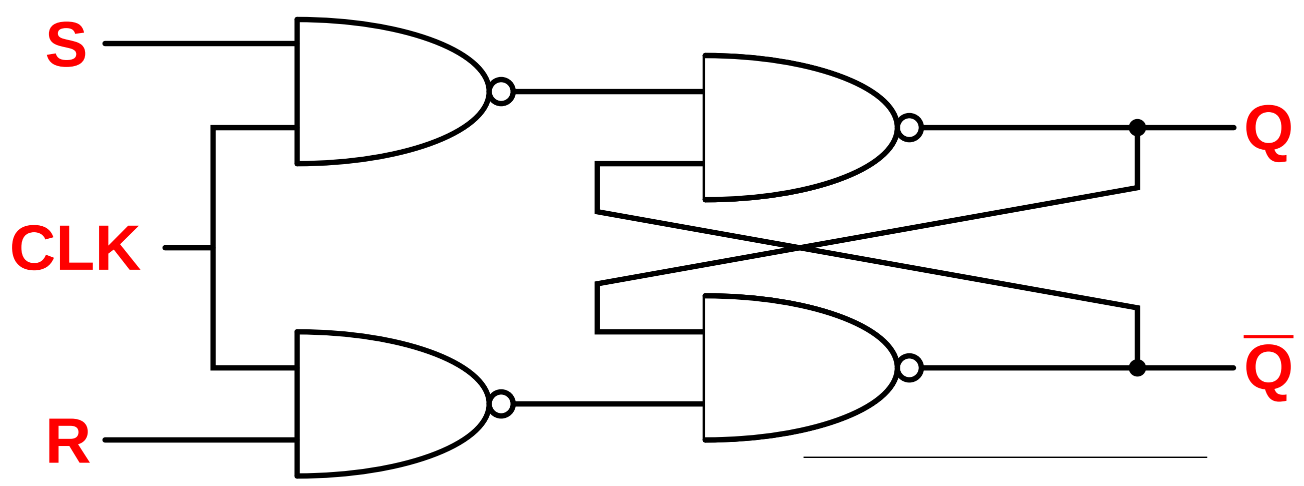


D	Q_{t+1}
1	0
0	1

D latch (transparent)

Some Issues

Forbidden FF states

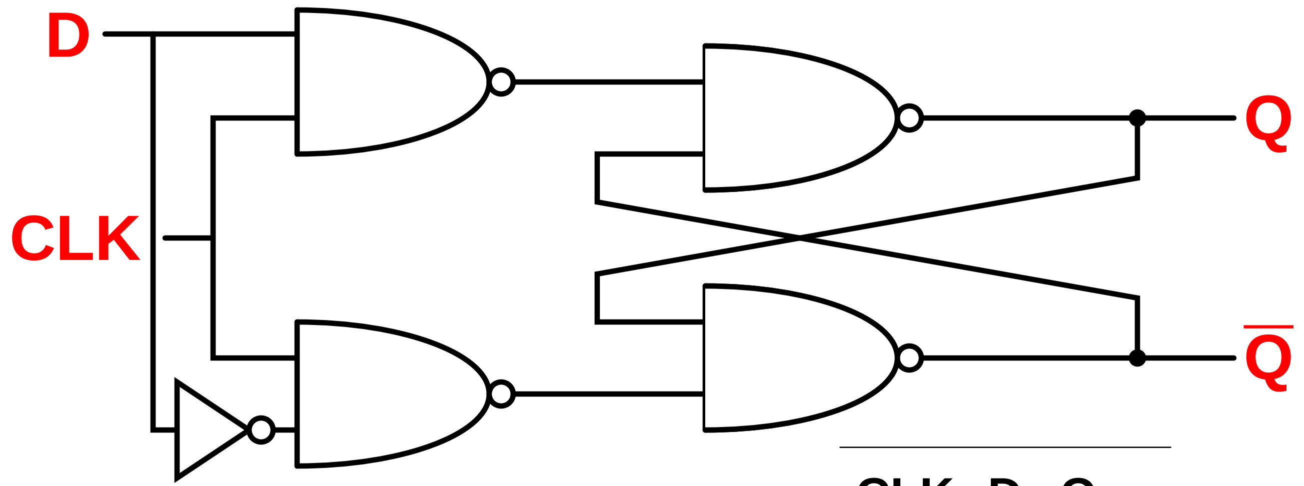


Gated SR latch (transparent)

CLK	S	R	Q_{t+1}
0	x	x	Q_t
1	0	0	Q_t
1	0	1	0
1	1	0	1
1	1	1	x

Some Issues

Forbidden FF states

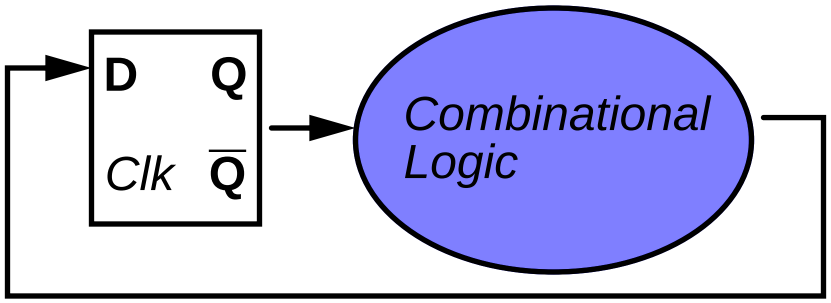


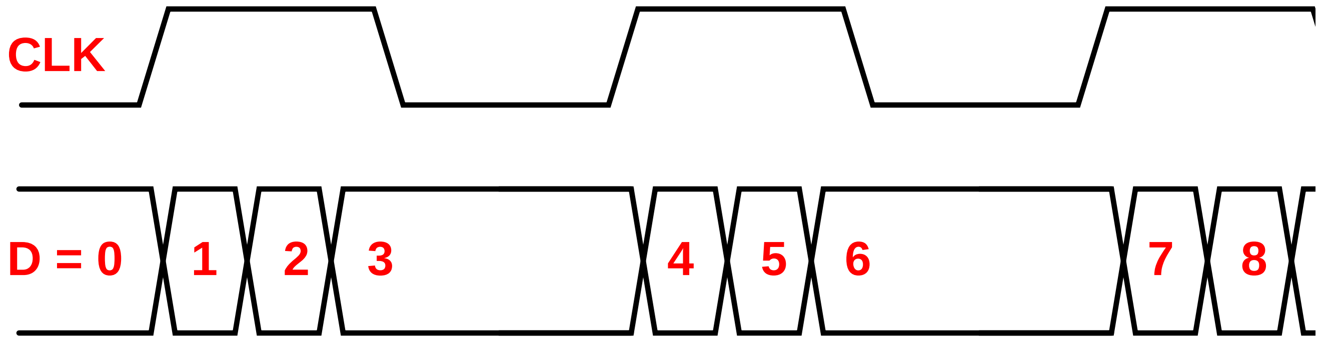
CLK	D	Q_{t+1}
0	x	Q_t
1	0	0
1	1	1

Gated D-latch (transparent)

Some Issues

Feed-through and race conditions

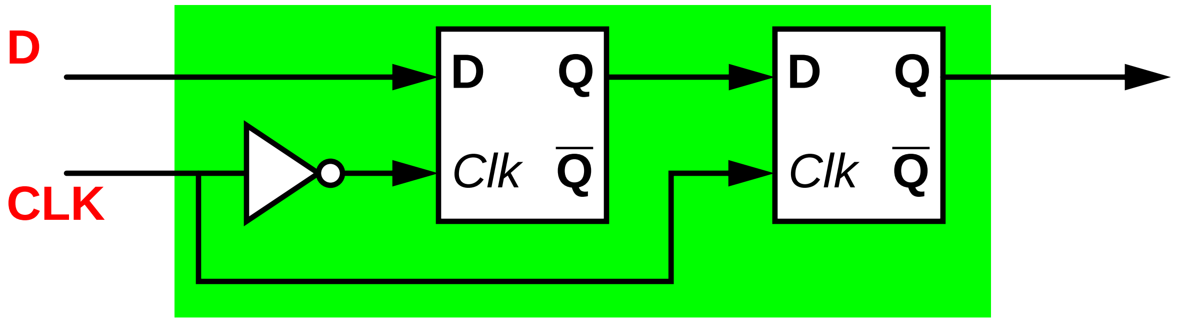




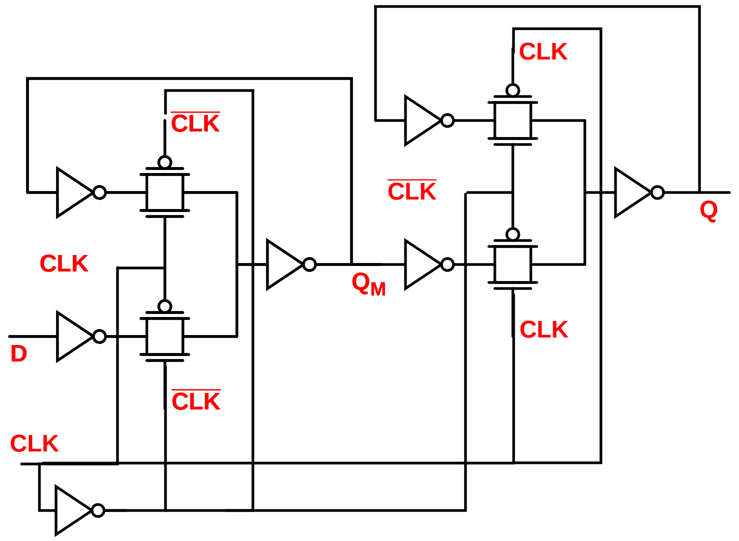
Transparent latches allow combinational logic *results* to be seen as its own *inputs*

Some Issues

Feed-through and race conditions



Master-slave D register (neg-edge triggered)



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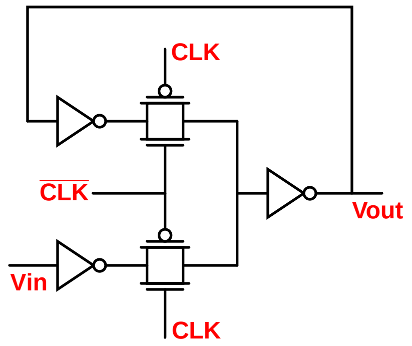
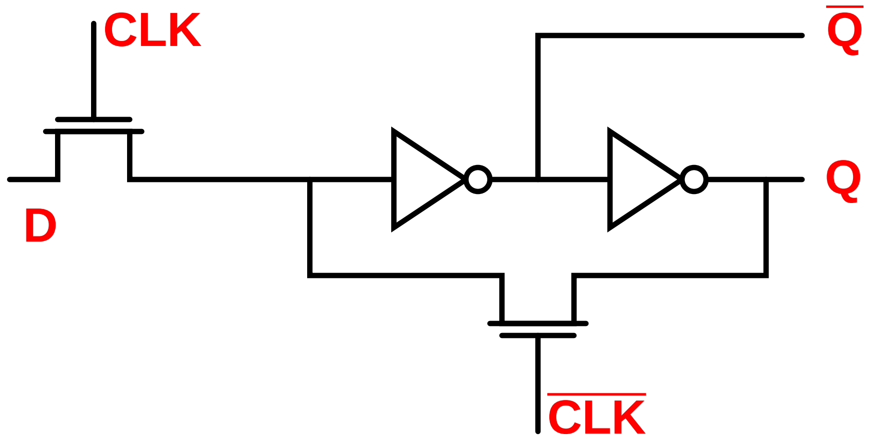
Some Issues

Cost of Clock Network (driving huge load)



Clock network drives 4 transistors per latch … power-expensive.

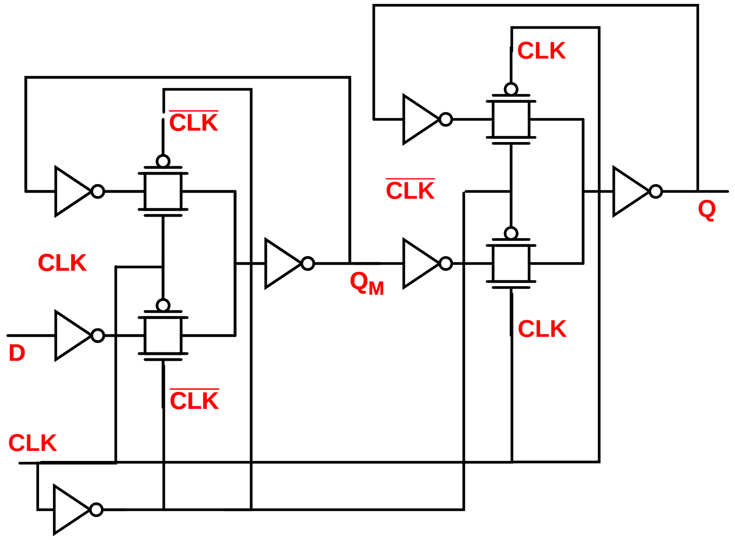
Alternative design:



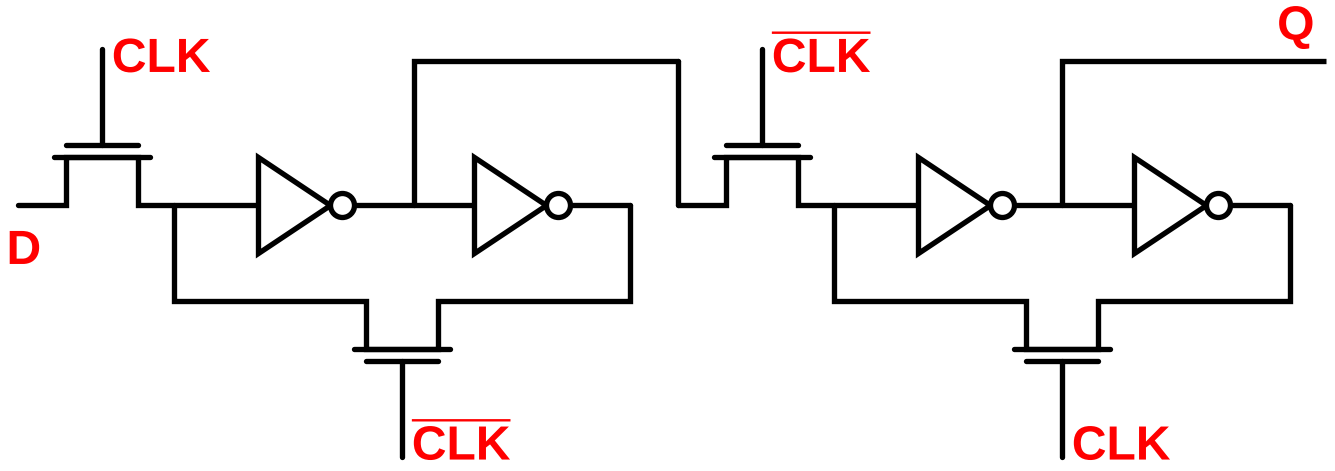
- Design w/ NMOS pass transistors presents smaller load to CLK; INV can recover low “1” but at a cost
- However: requires non-overlapping CLK/$\overline{\text{CLK}}$ … why?

Some Issues

Cost of Clock Network (driving huge load)



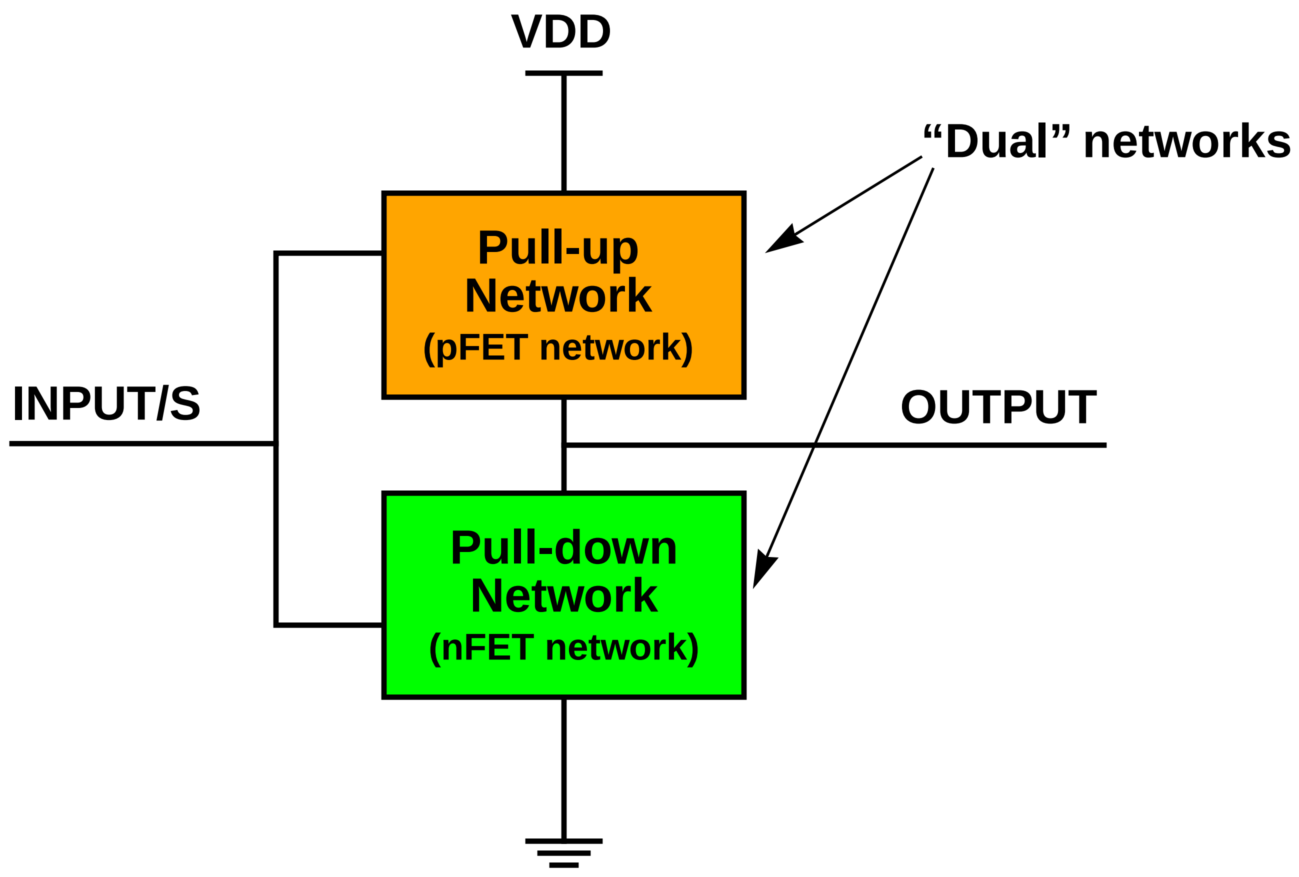
Similar example, with master-slave organzation



Some Issues

Number of Transistors: Dynamic Logic

(first: Primer … recall complementary logic)



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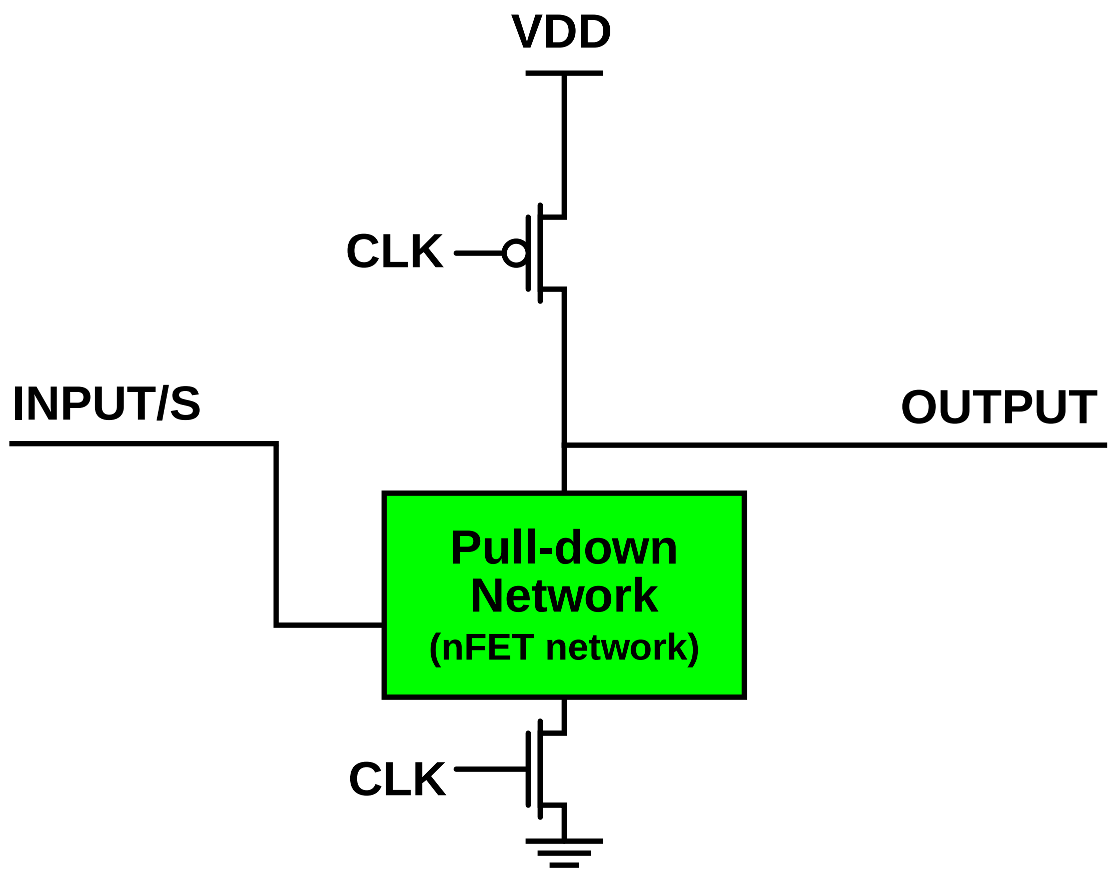
Some Issues

Number of Transistors: Dynamic Logic

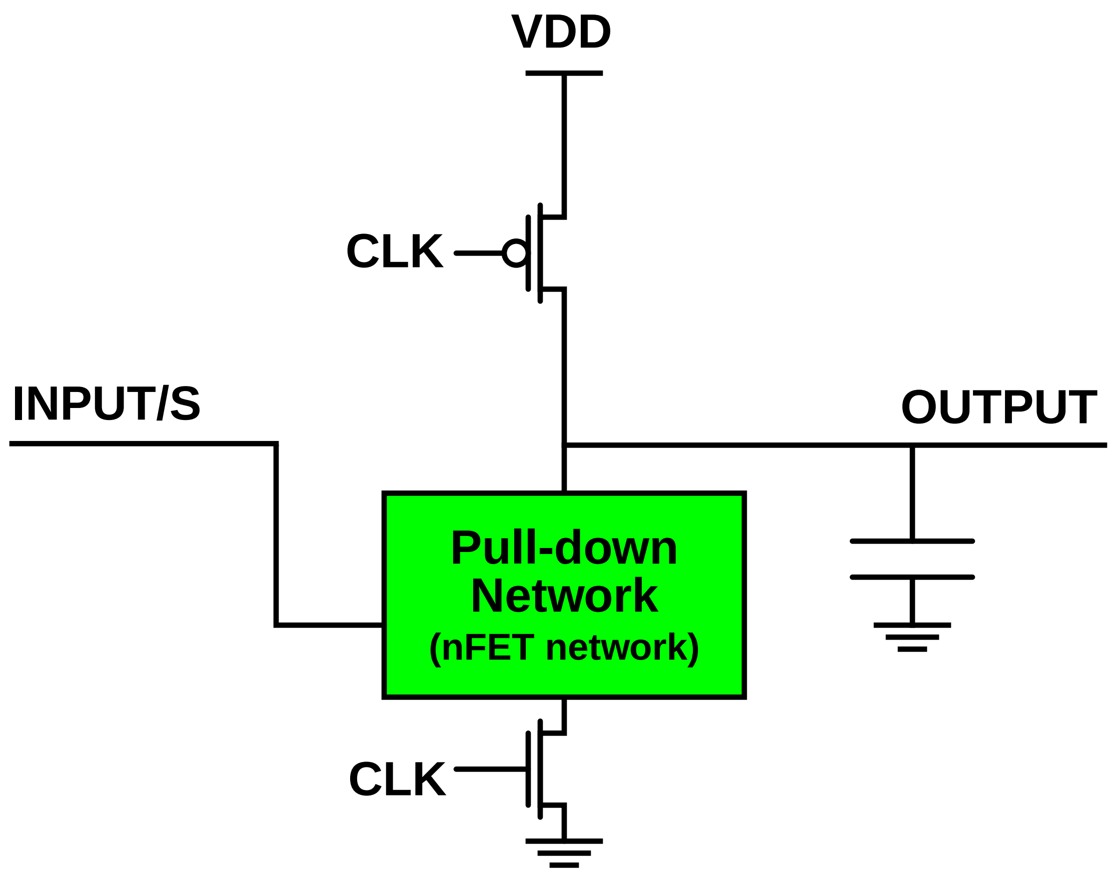
(… no longer complementary …)



Some Issues

Number of Transistors: Dynamic Logic

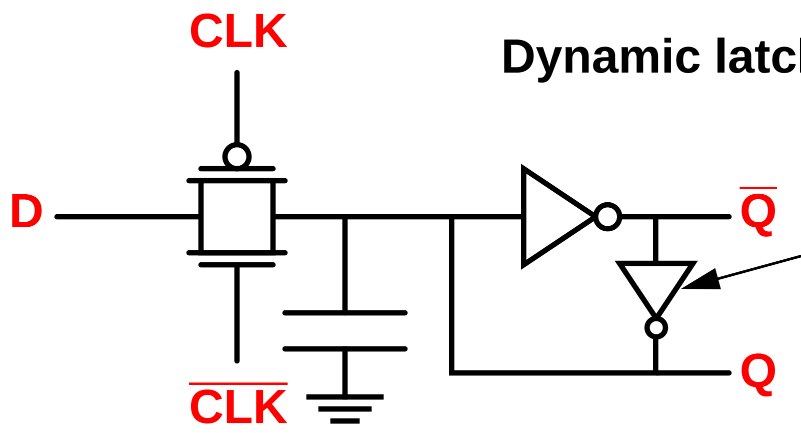
(… relies upon capacitance, burns power)



Some Issues

Number of Transistors: *Dynamic* Storage

Dynamic latch (transparent)

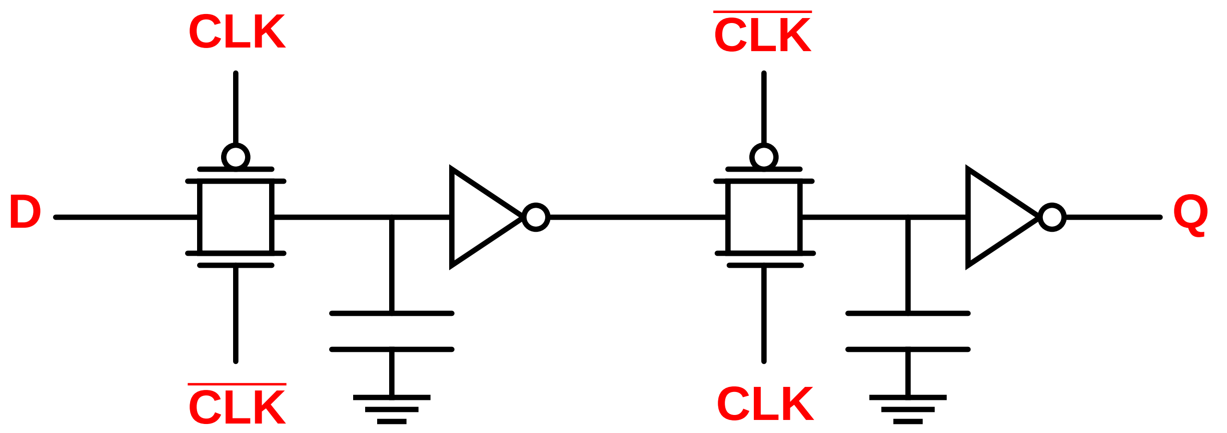


Create “pseudostatic” latch:

Make this inverter weak so that D input overpowers feedback loop.

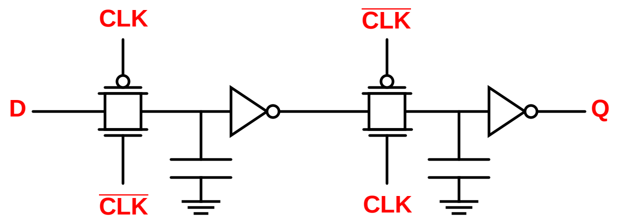
How to make weak inverter:
W/L: make W small or L large

Dynamic edge-triggered register



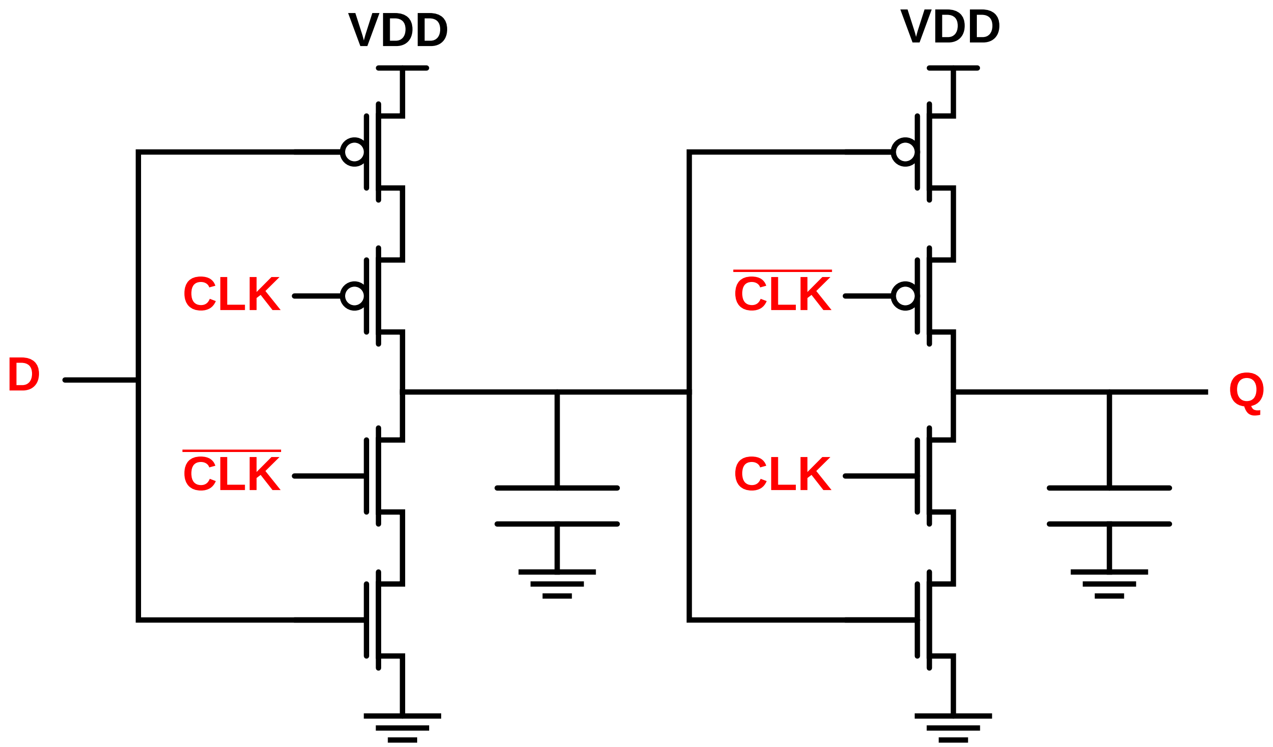
Some Issues

Non-overlapping clocks: Clocked CMOS



This allows feed-through when clocks overlap.

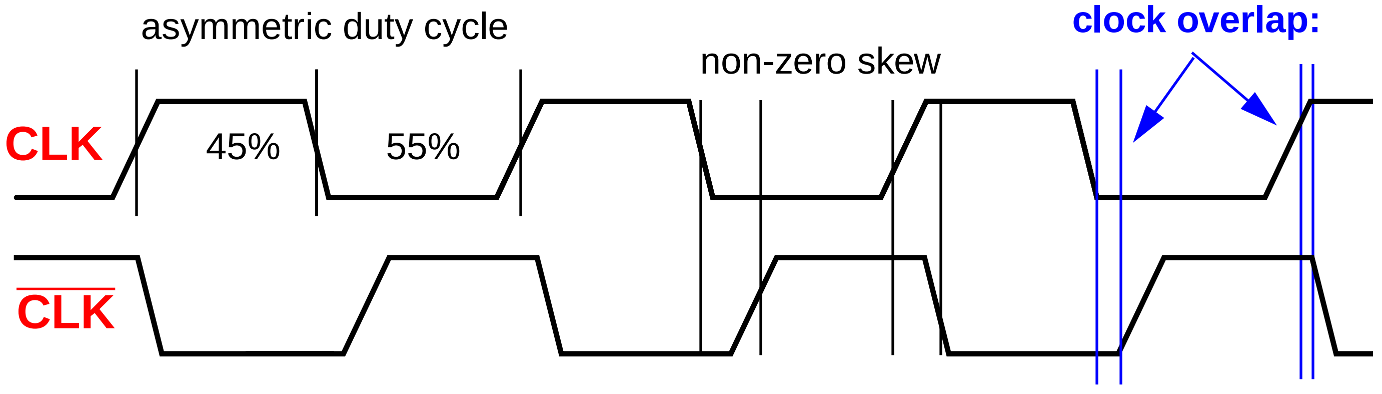
This design does not:

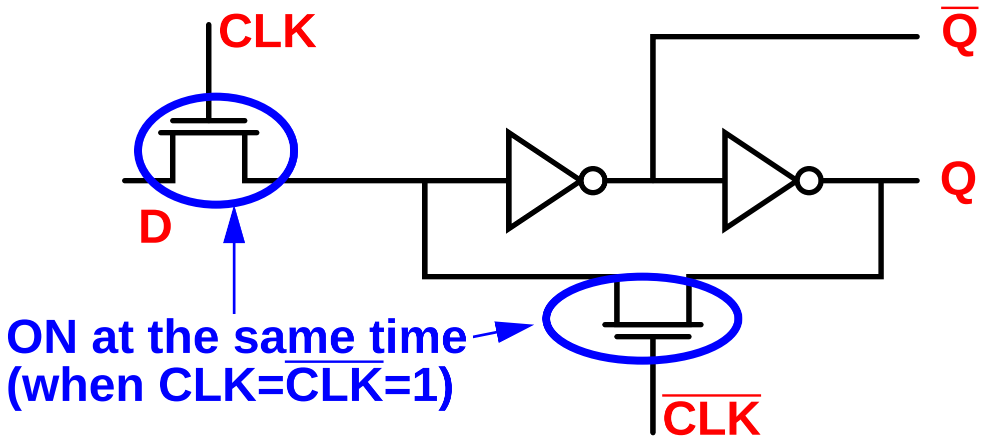


Some Issues

Non-overlapping clocks: Clocked CMOS

EXAMPLES:





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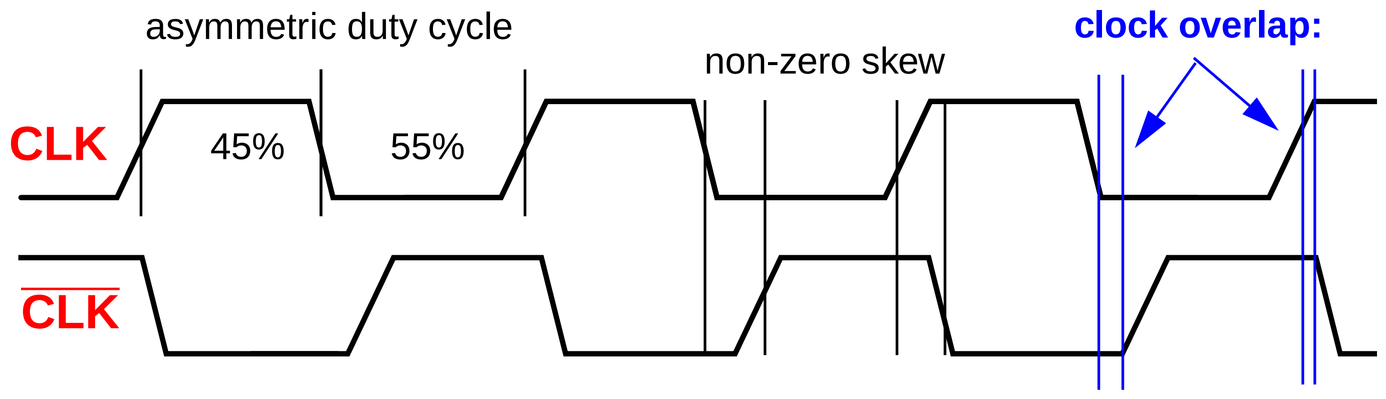
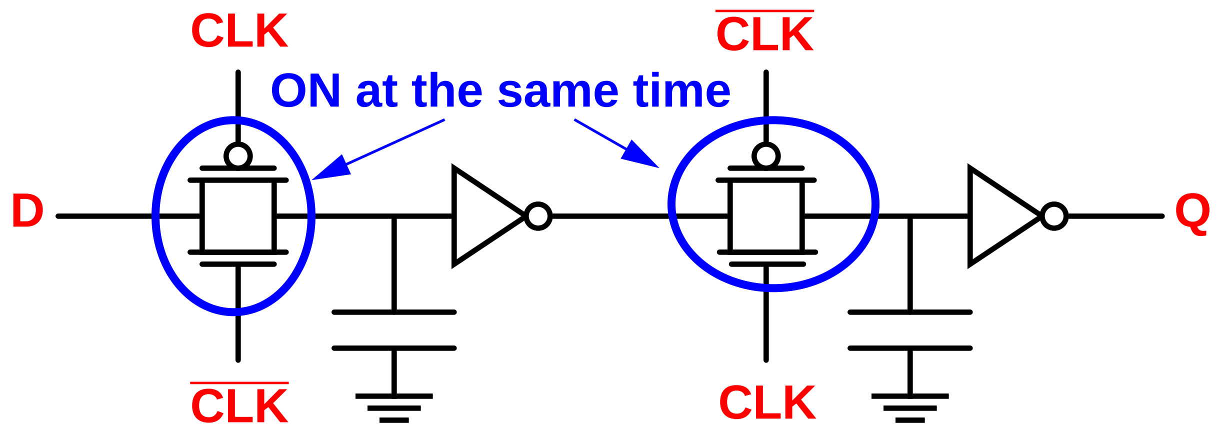
Some Issues

Non-overlapping clocks: Clocked CMOS

EXAMPLES:

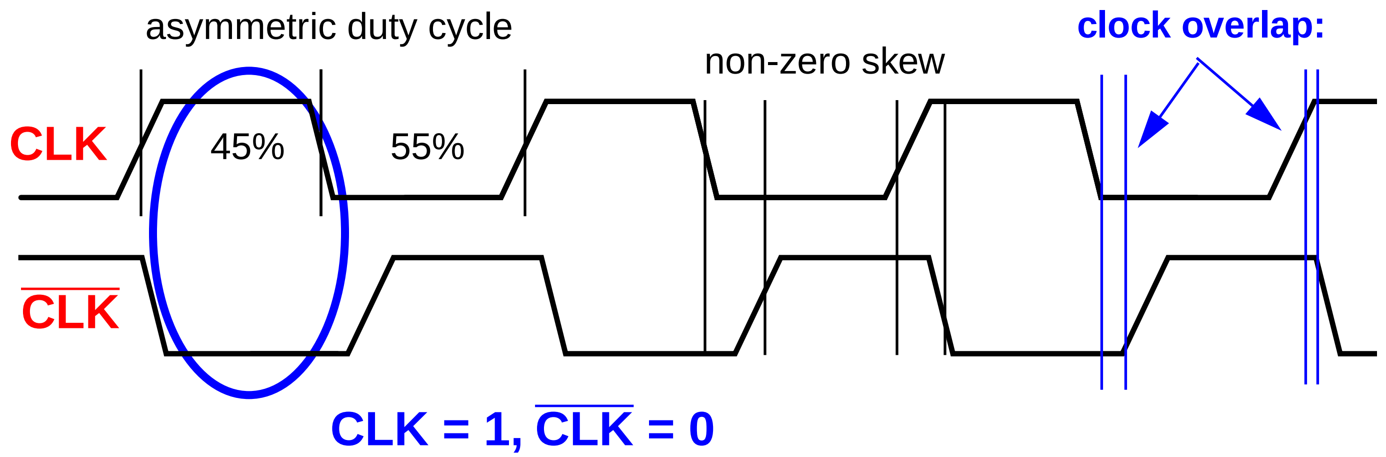


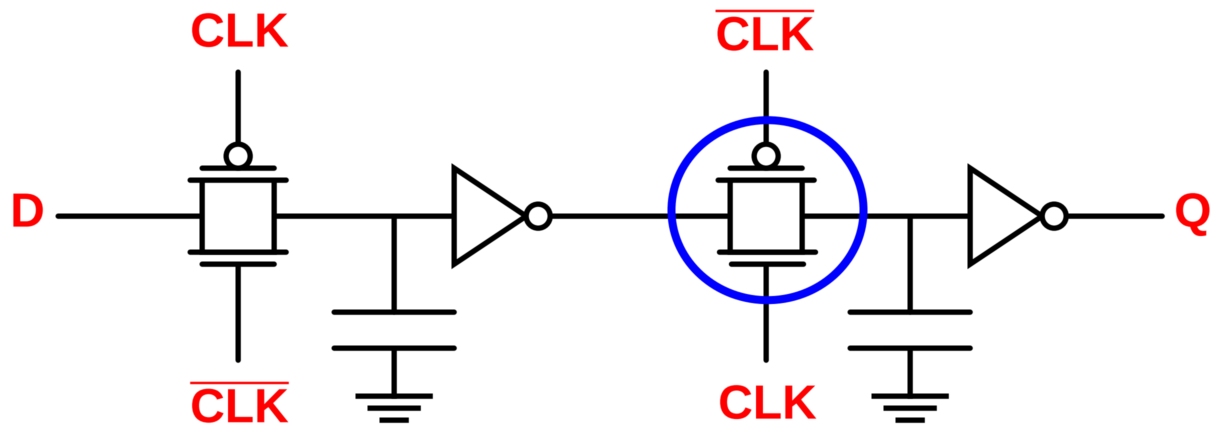


Some Issues

Non-overlapping clocks: Clocked CMOS

EXAMPLES:





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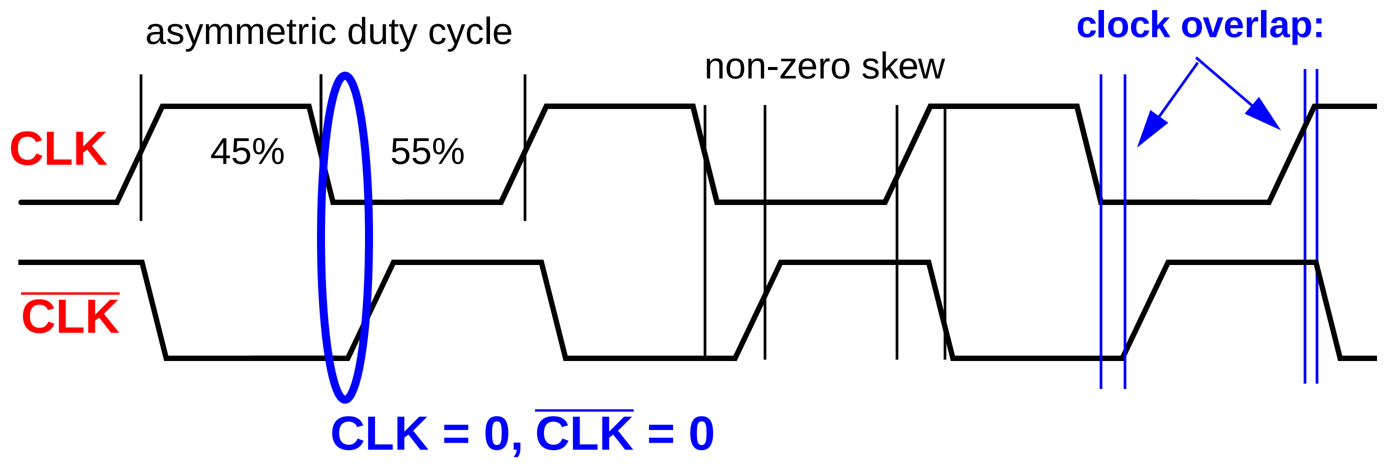
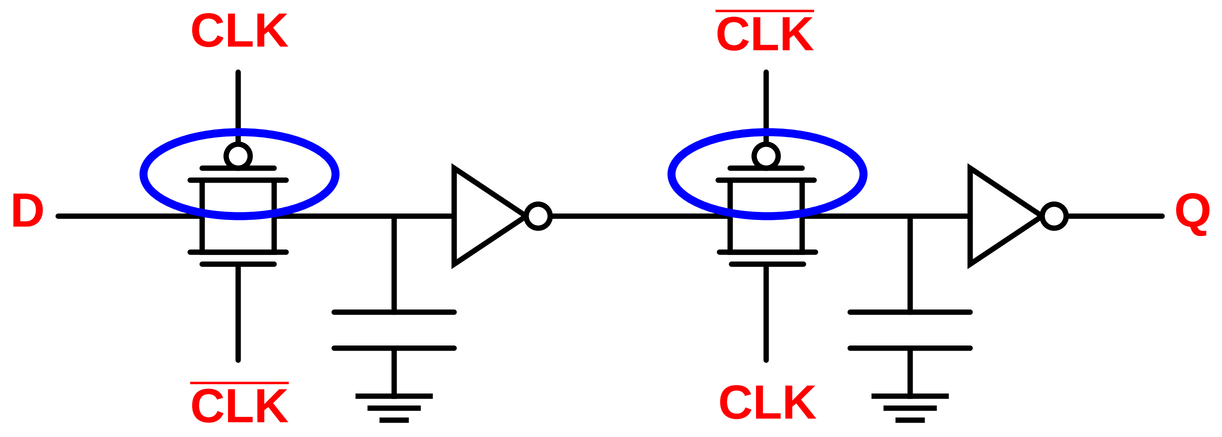
Some Issues

Non-overlapping clocks: Clocked CMOS

EXAMPLES:

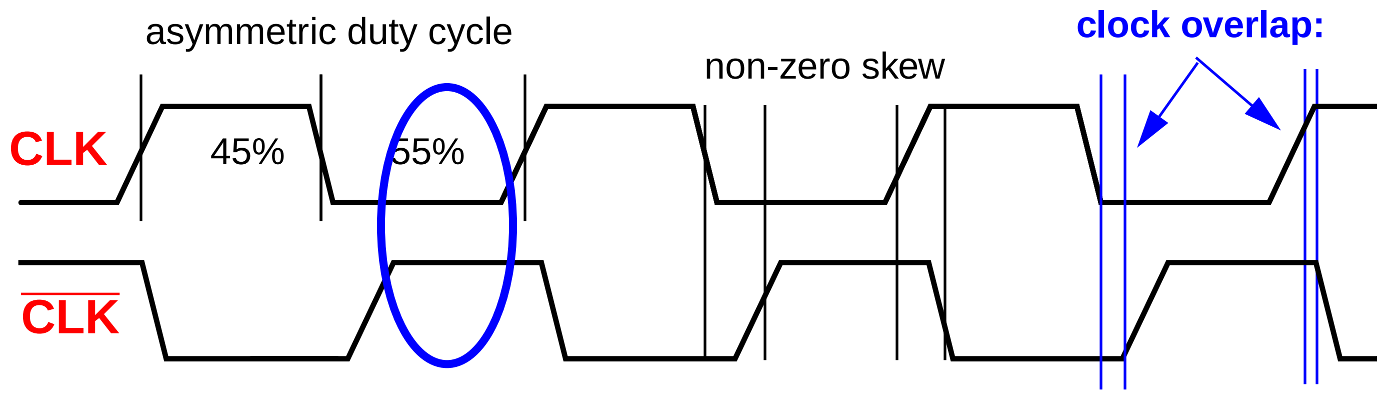




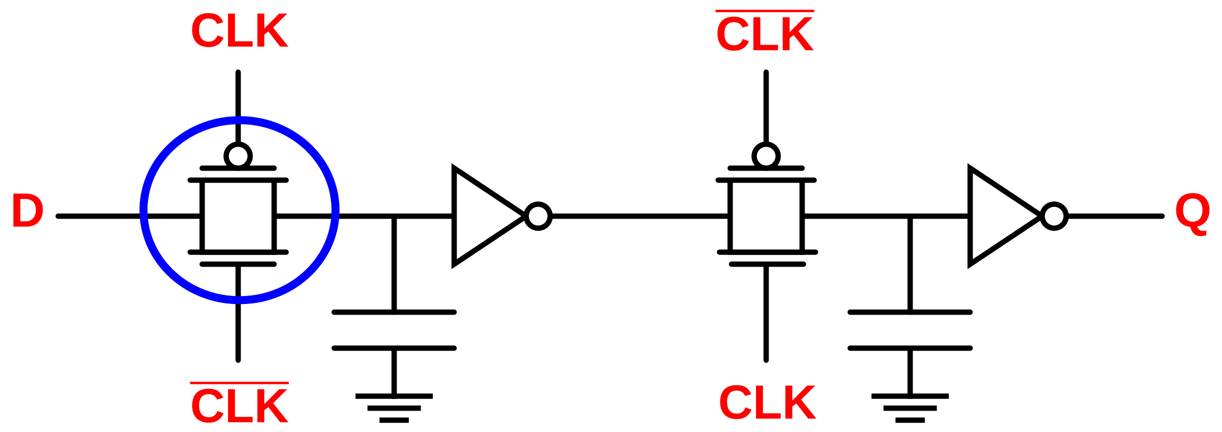
Some Issues

Non-overlapping clocks: Clocked CMOS

EXAMPLES:



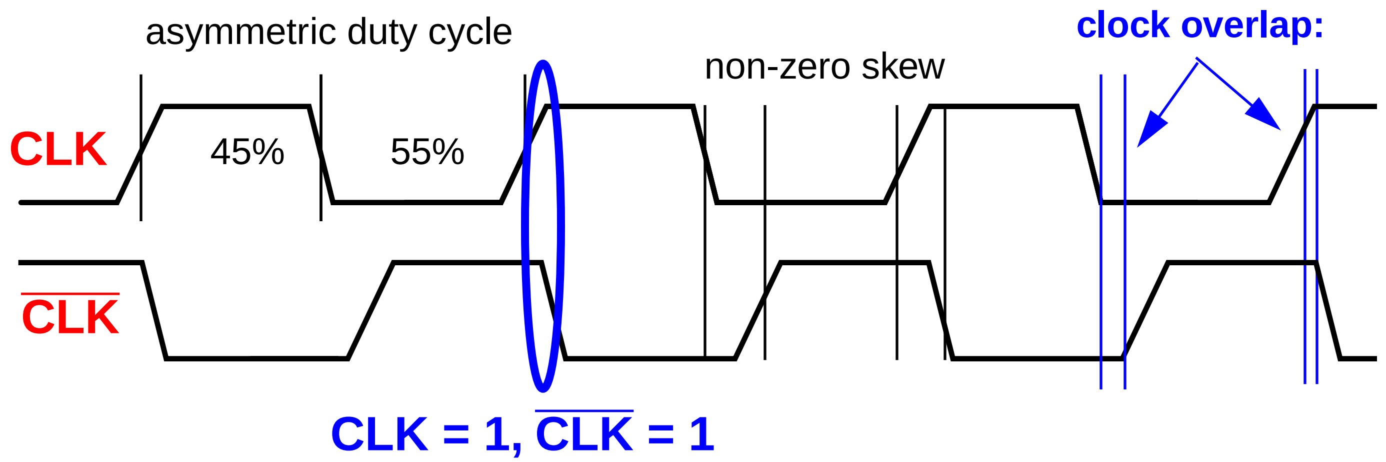
$\text{CLK} = 0, \overline{\text{CLK}} = 1$

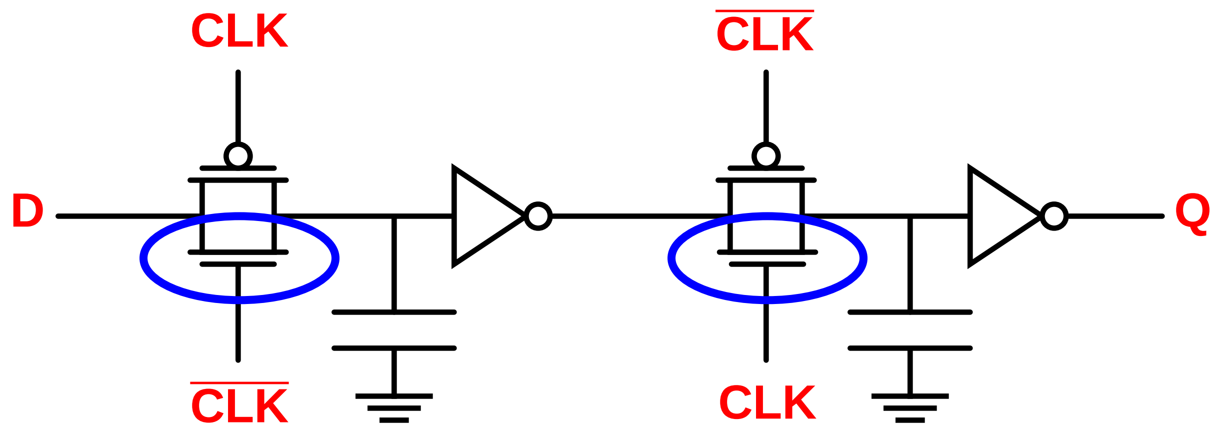


Some Issues

Non-overlapping clocks: Clocked CMOS

EXAMPLES:





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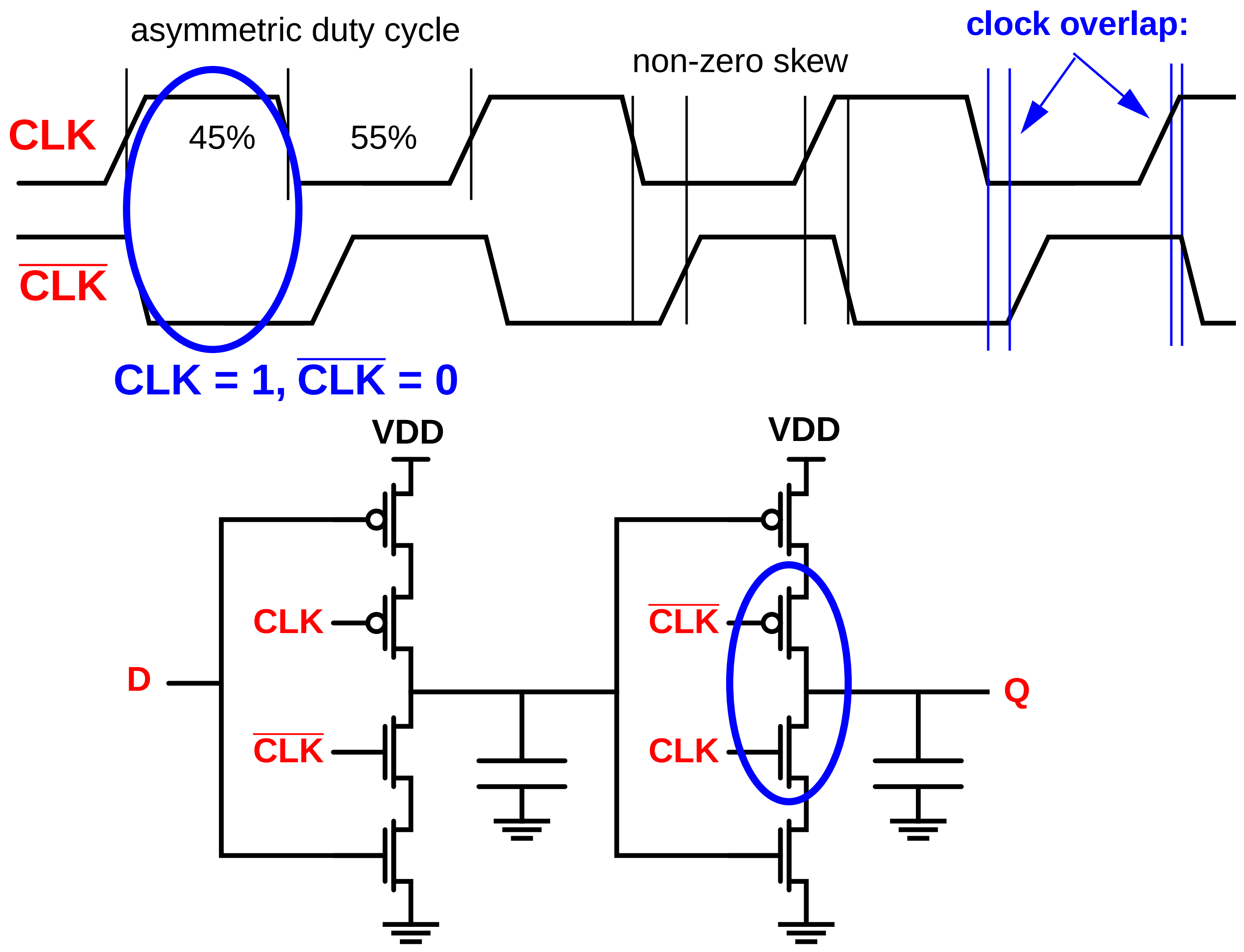
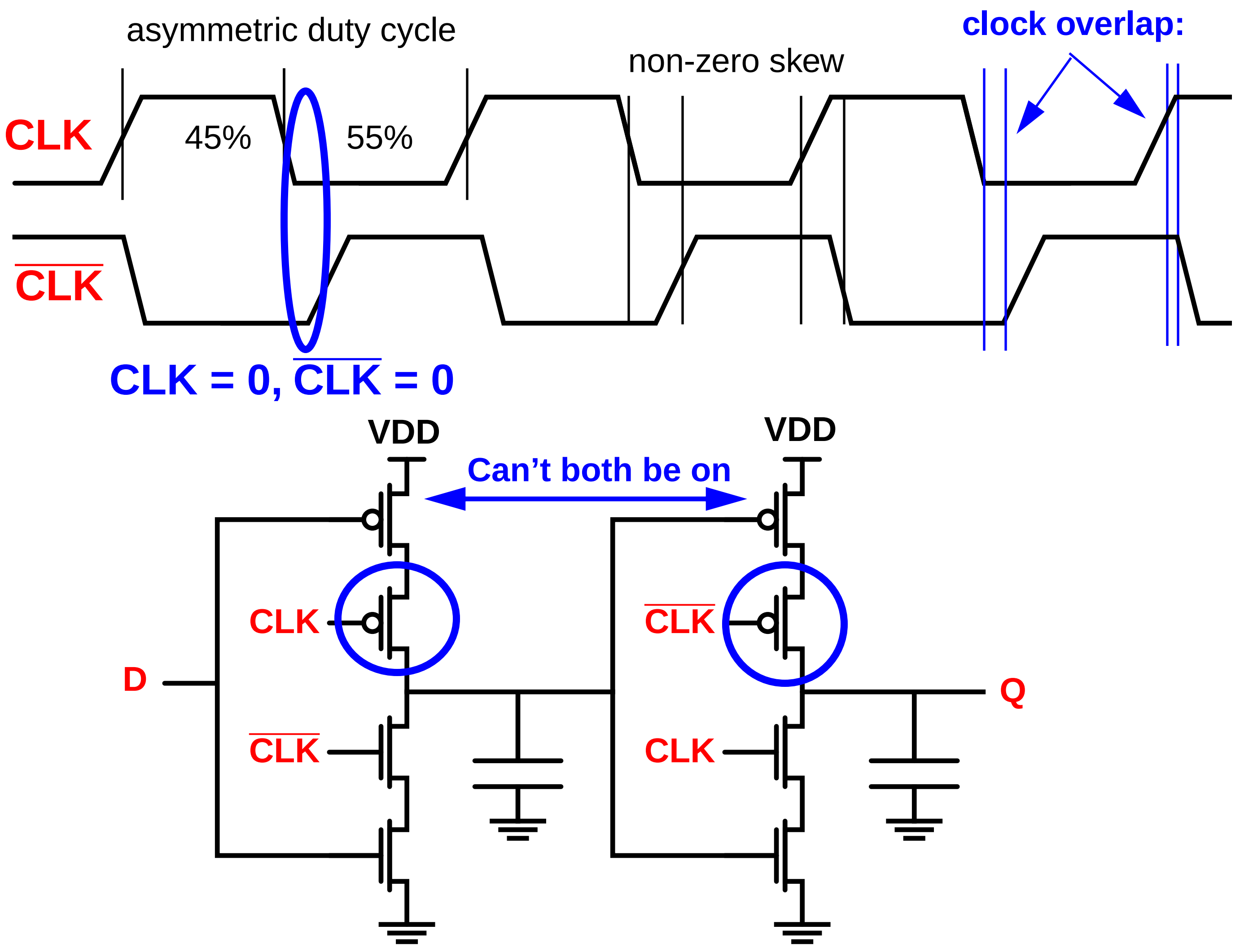
Some Issues

Non-overlapping clocks: Clocked CMOS



Some Issues

Non-overlapping clocks: Clocked CMOS



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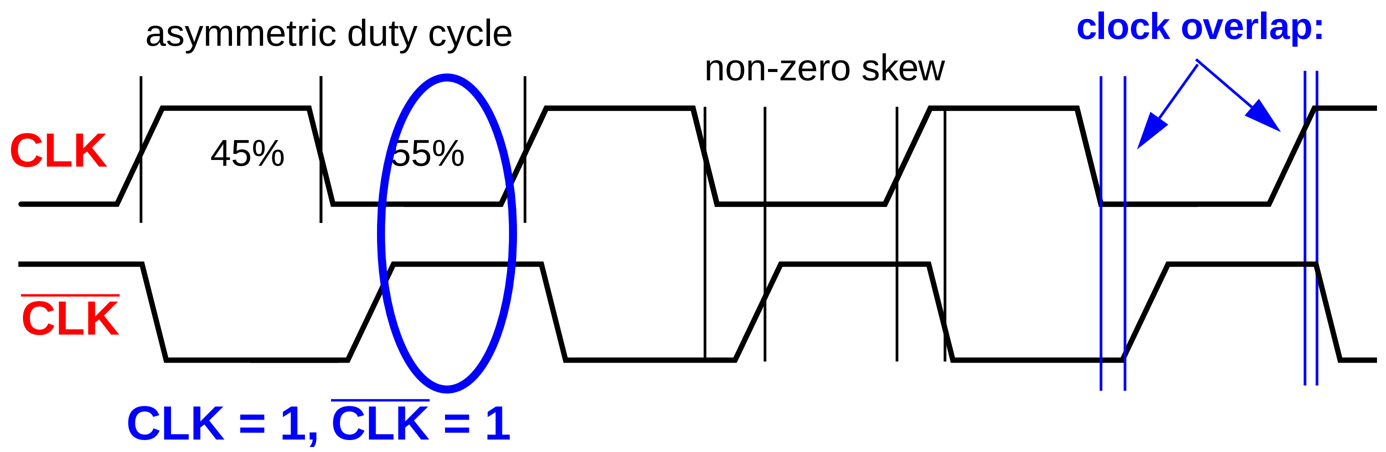
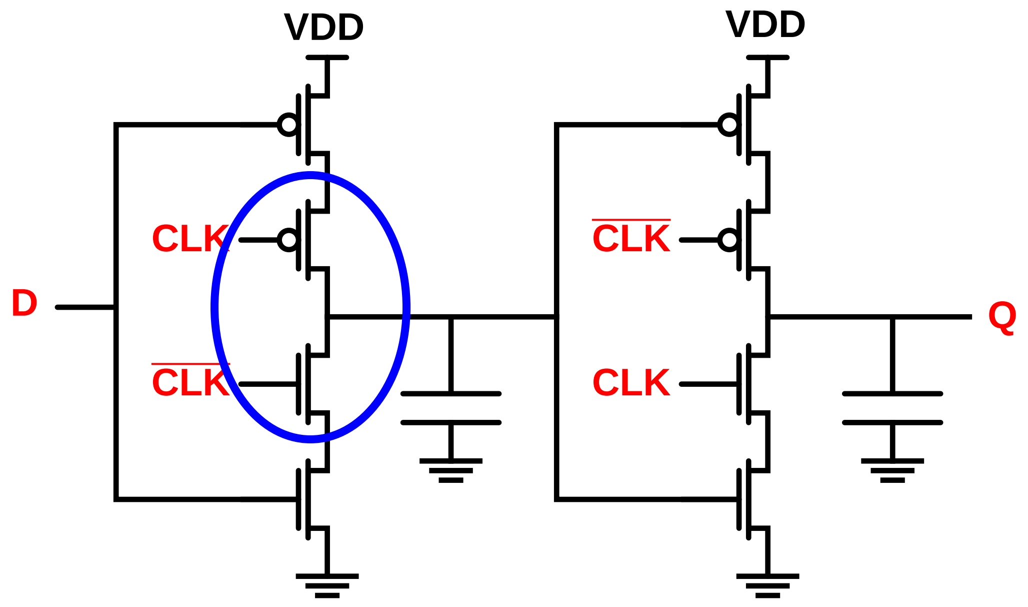
Some Issues

Non-overlapping clocks: Clocked CMOS





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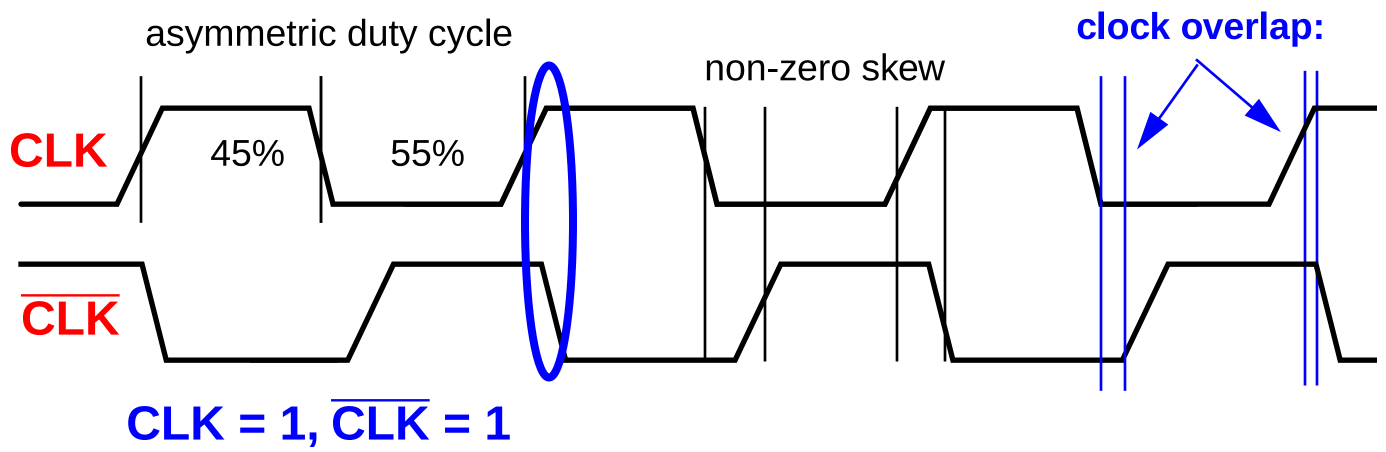
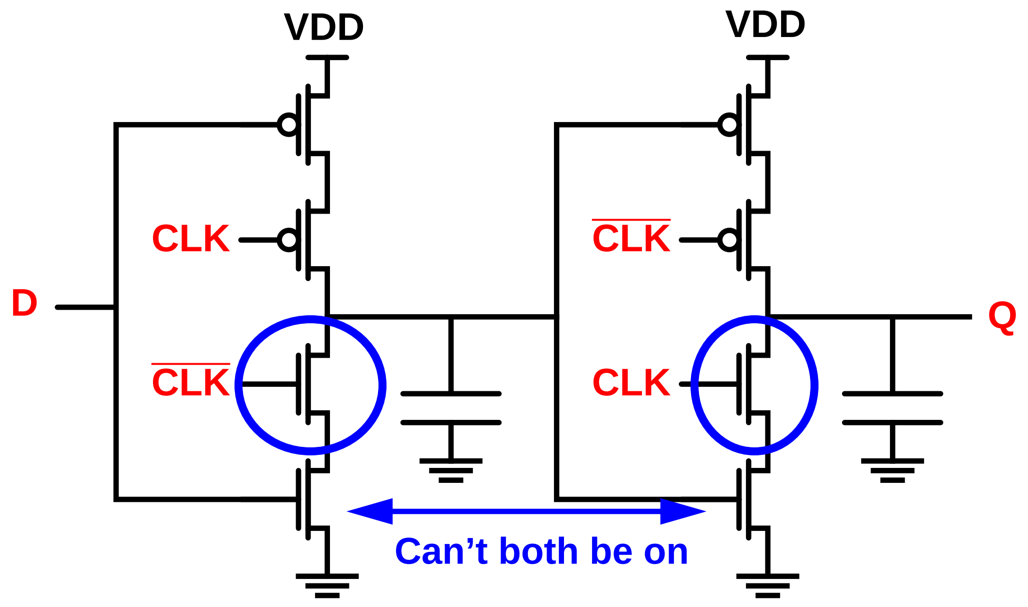
Some Issues

Non-overlapping clocks: Clocked CMOS





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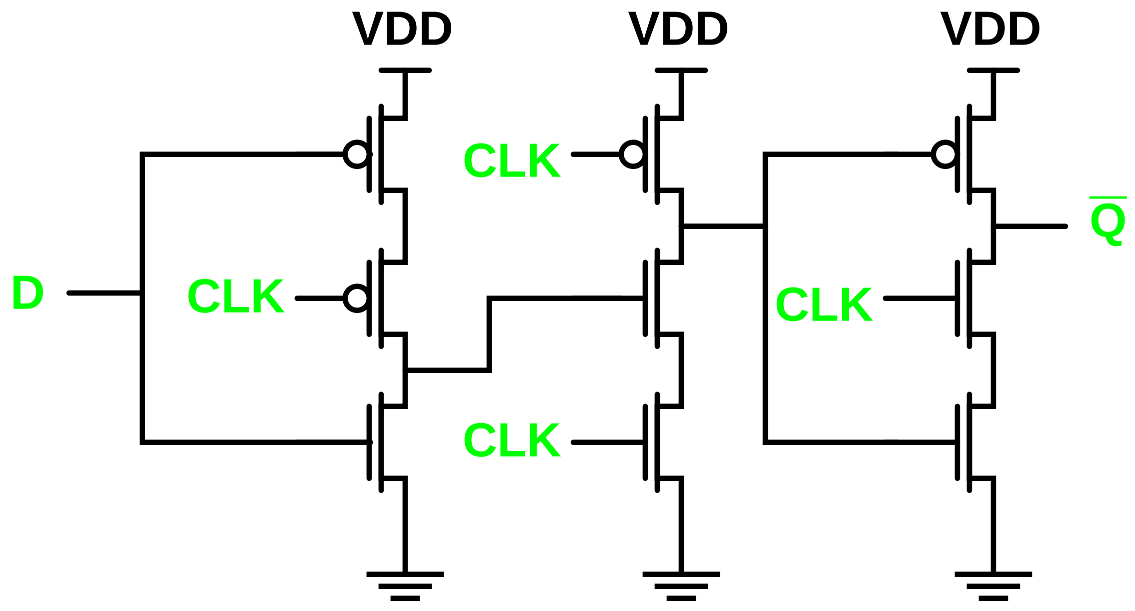
Some Issues

Non-overlapping clocks:

“True” Single-Phase Clocked Register

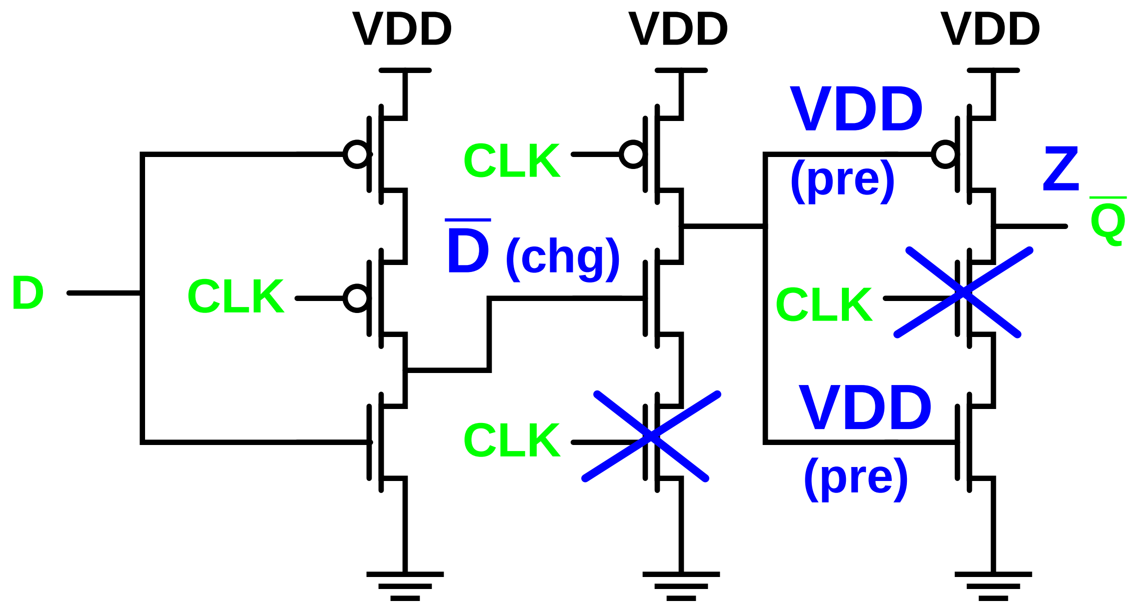


Positive edge-driven register

Some Issues

Non-overlapping clocks:

“True” Single-Phase Clocked Register



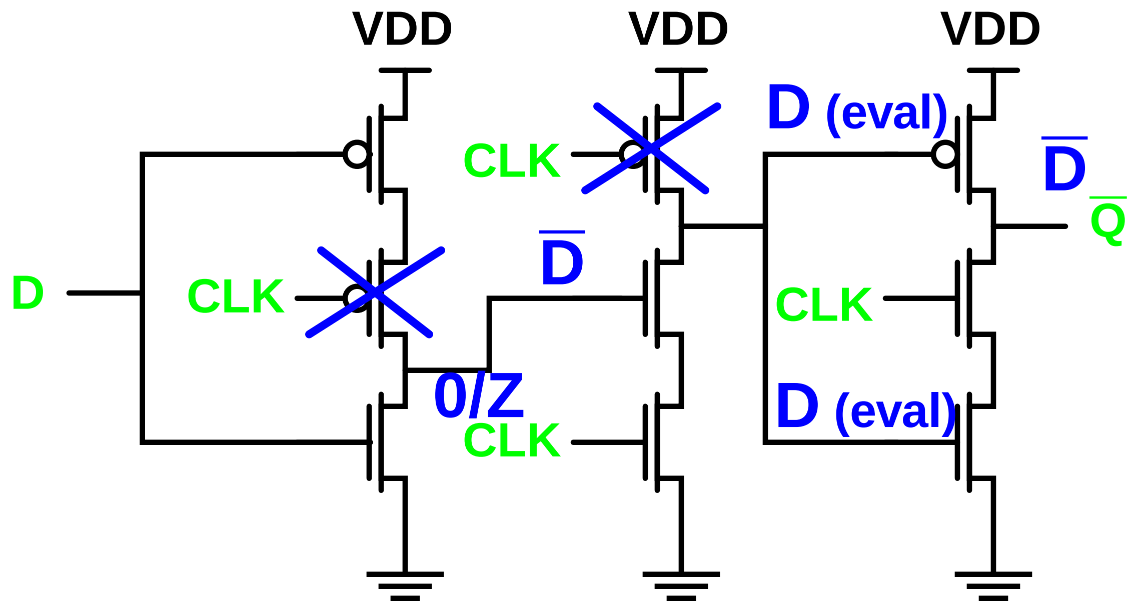
CLK = 0

Output = Z => output is *stable* (dynamic)

Some Issues

Non-overlapping clocks:

“True” Single-Phase Clocked Register

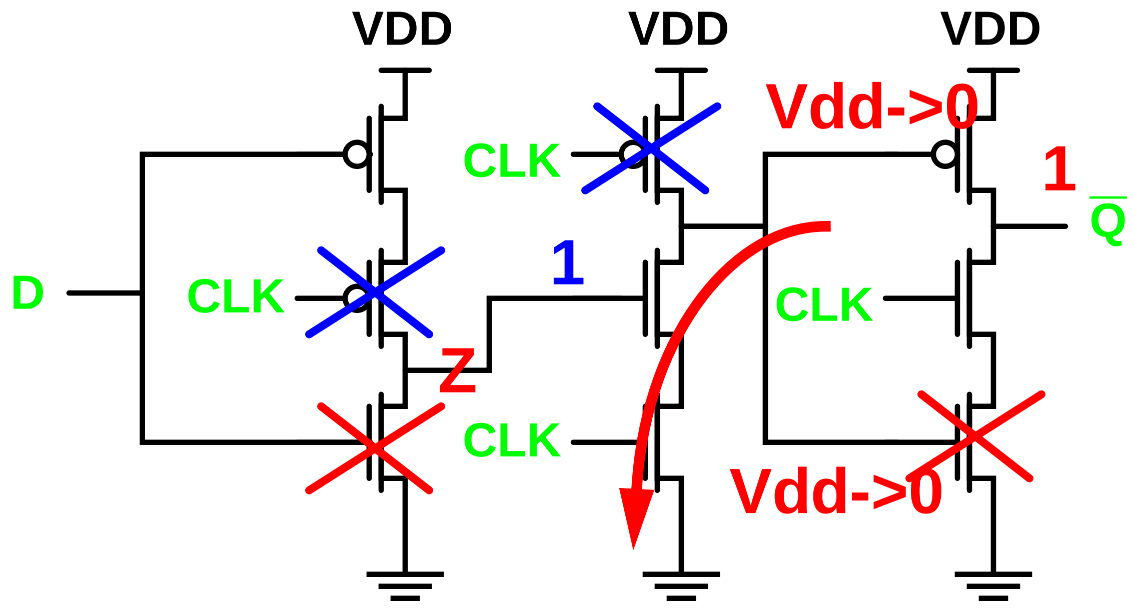


CLK = 1

Some Issues

Non-overlapping clocks:

“True” Single-Phase Clocked Register

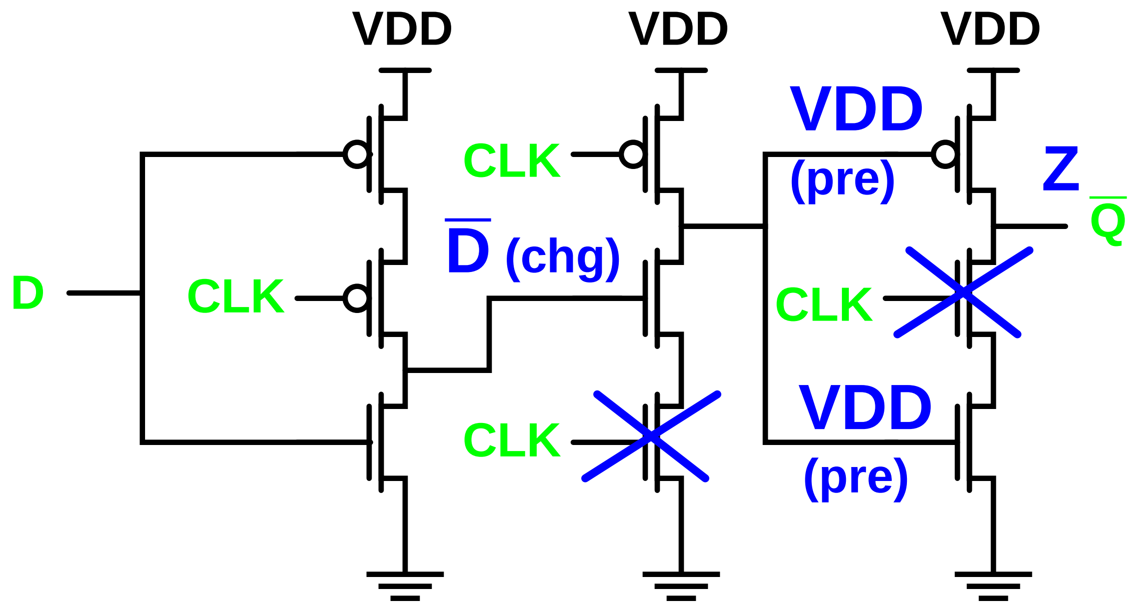


CLK = 1, D = 0

Some Issues

Non-overlapping clocks:

"True" Single-Phase Clocked Register

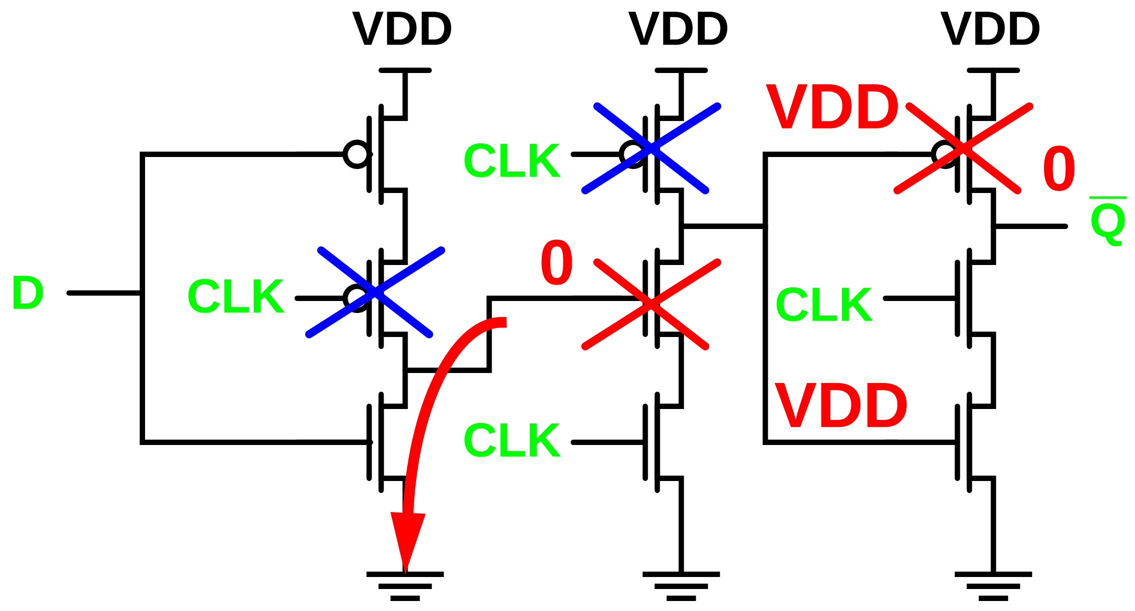


CLK = 0

Some Issues

Non-overlapping clocks:

“True” Single-Phase Clocked Register



CLK = 1, D = 1

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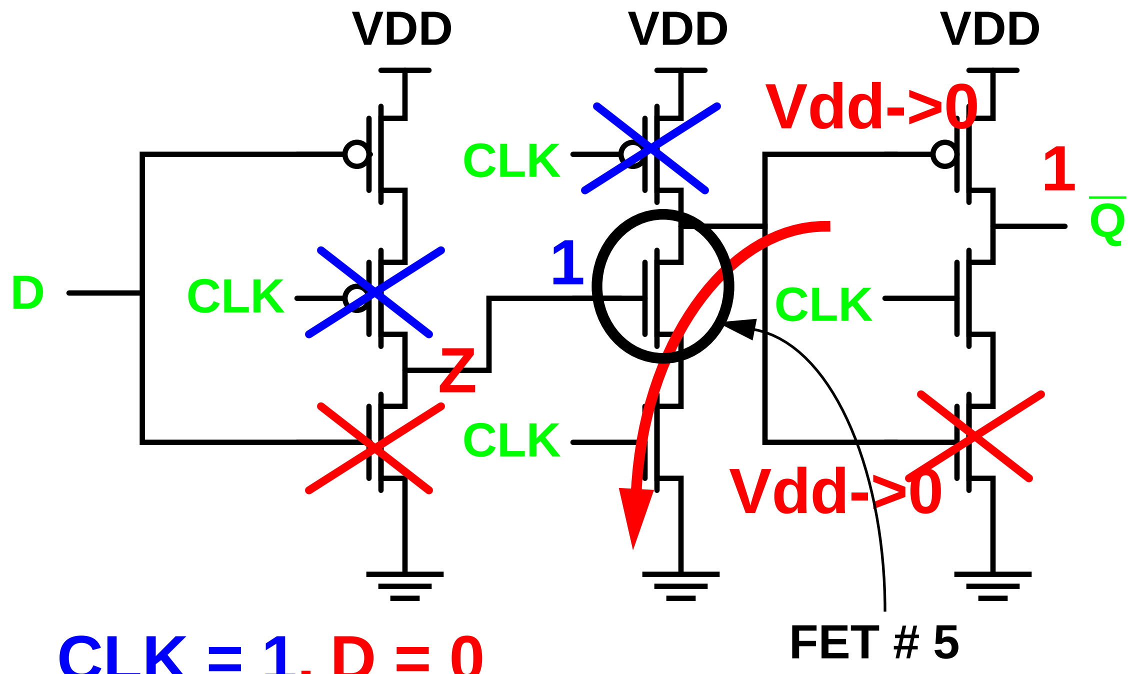
Some Issues

Non-overlapping clocks:
"True" Single-Phase Clocked Register



CLK = 1, D = 0

Note: if D is allowed to transition from 0 to 1 too soon after CLK transitions 0->1, it is possible to close FET #5 before the final capacitance discharges (Vdd -> 0) … which would obviously pose a problem.

This represents the *hold time* of this register.

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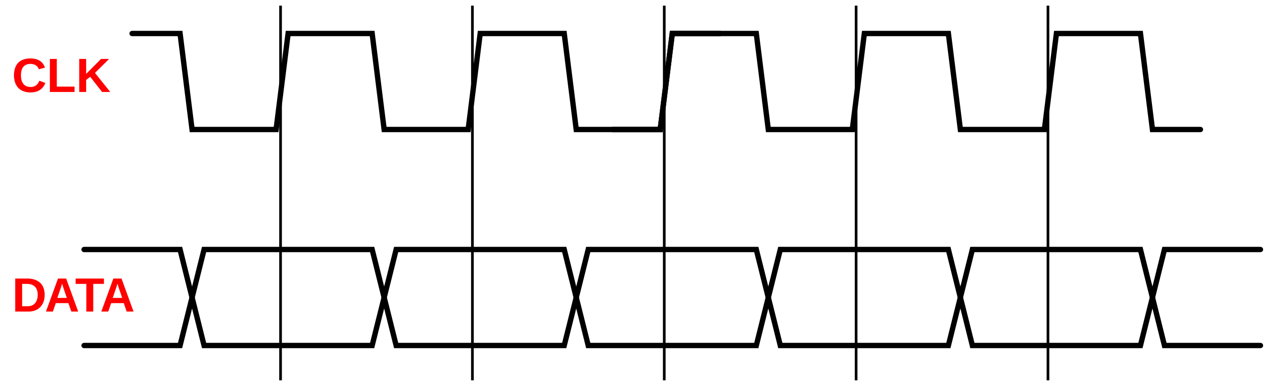
Some Issues

Clock power: Dual-Edge-Triggered Reg.



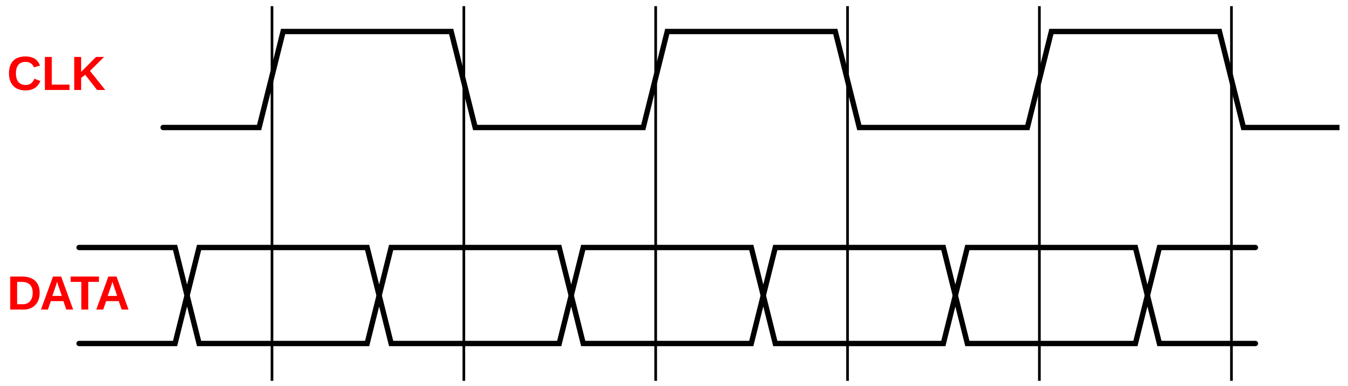
Note that clock transitions twice as often as data does (actually, even more, unless the data pattern happens to be 01010101010 …)

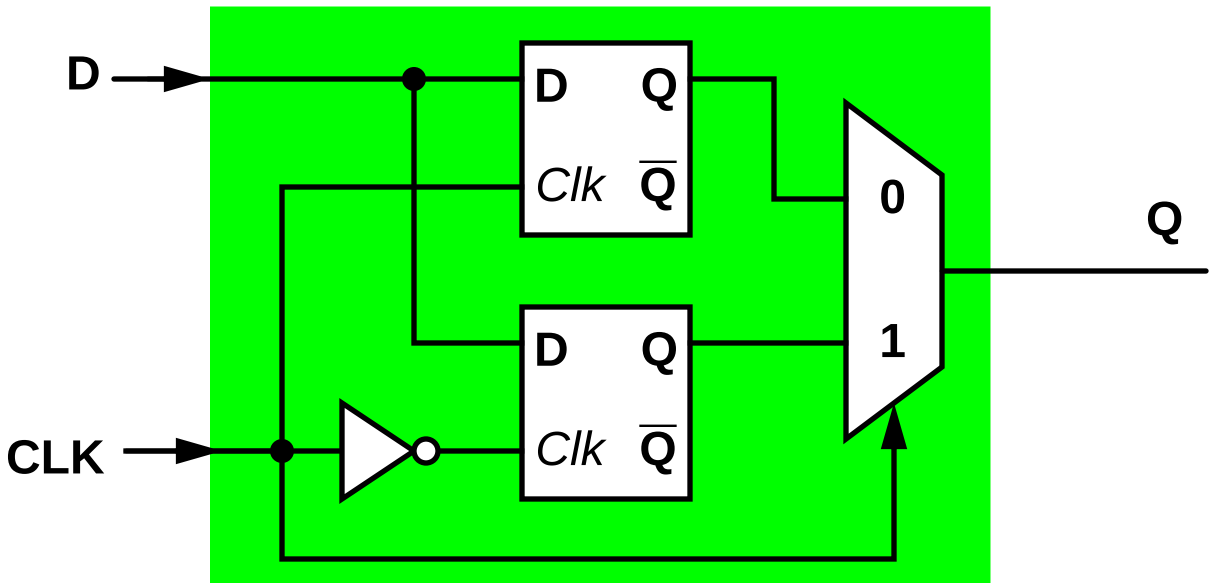
Max data rate = 1Gbps; clock rate = 2GHz

At high frequencies, this is a problem

Some Issues

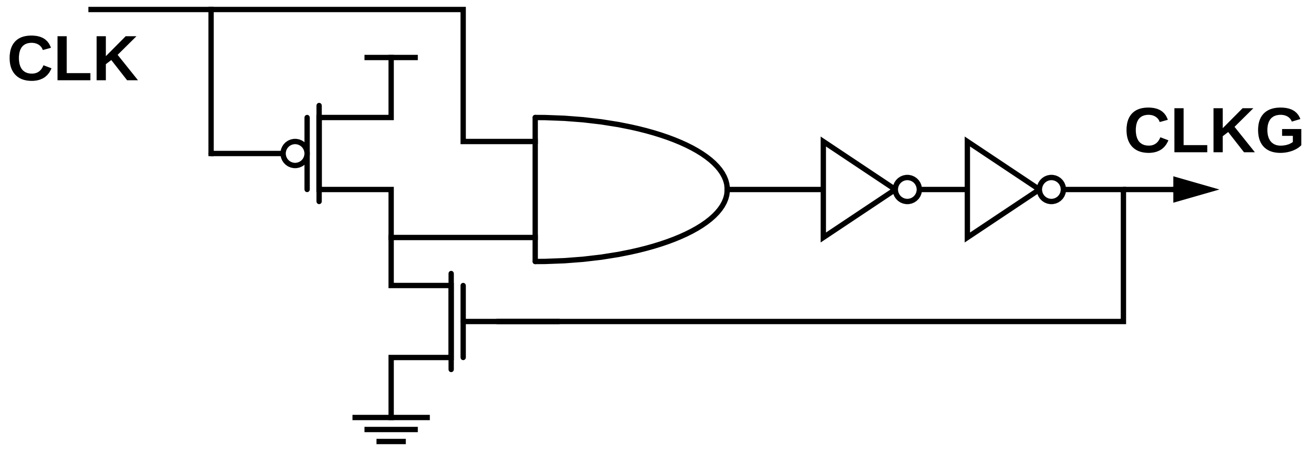
Clock power: Dual-Edge-Triggered Reg.

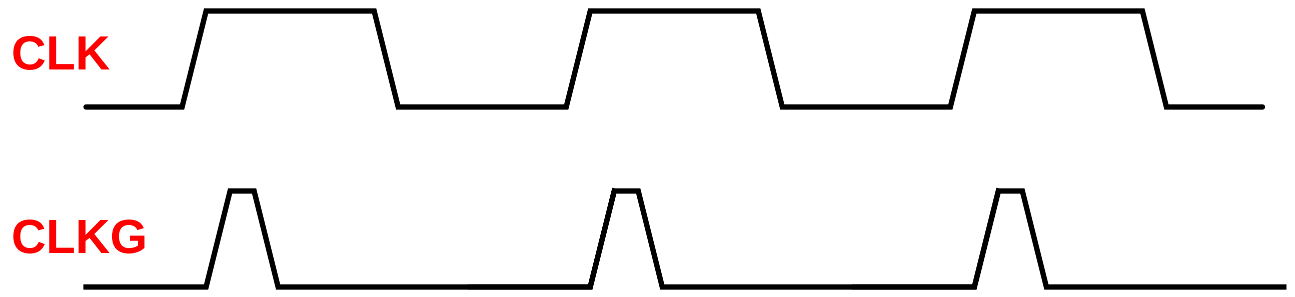




Some Issues

Simplicity, speed of design: Pulse registers





For use with transparent latches: creates *de facto* registers, provided you do thorough timing analysis to guarantee inputs to latch stable during transparent window.

Benefits: latches much faster than registers, use fewer transistors, present lighter load to clock network (leads to lower power consumption).

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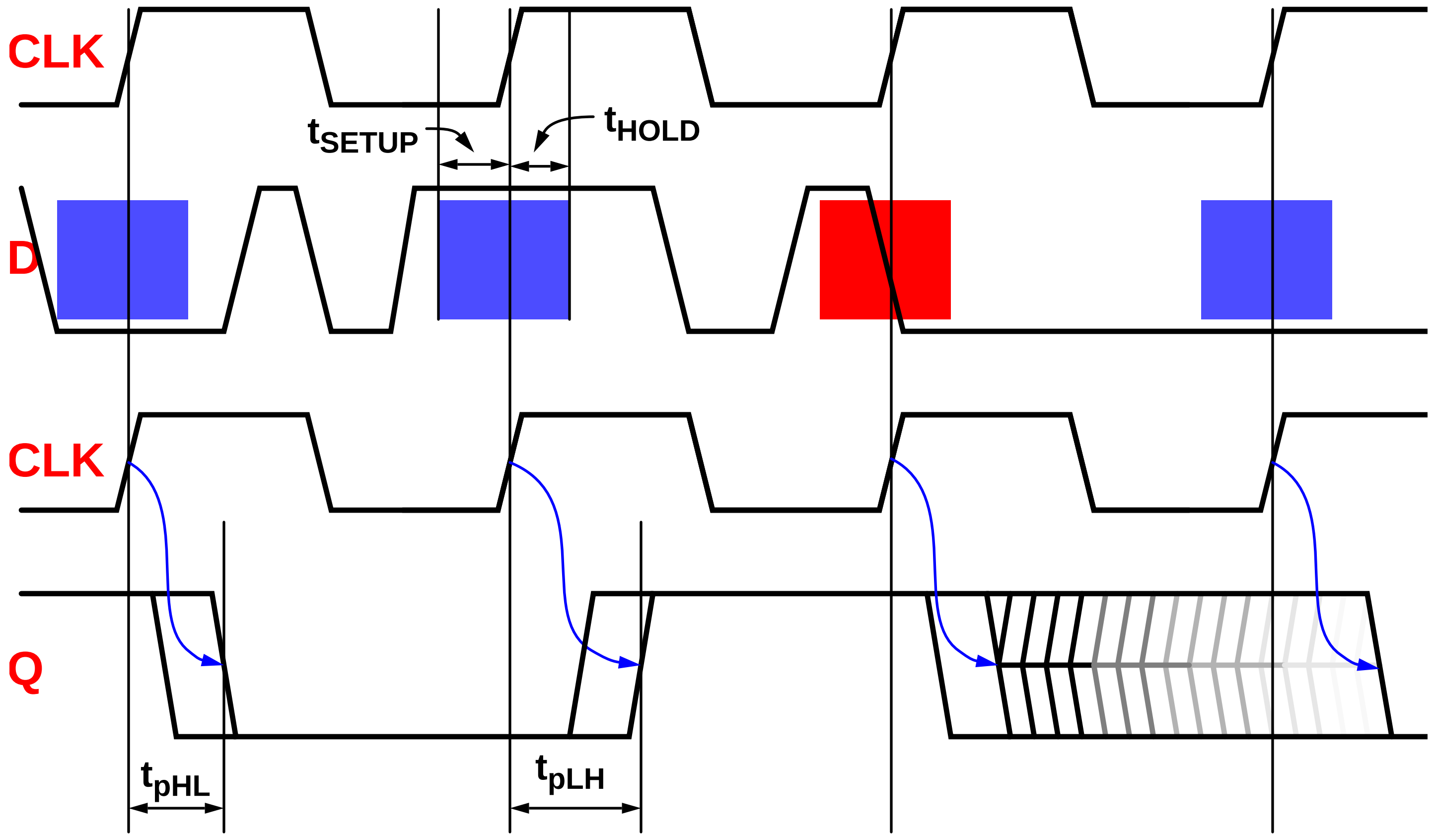
Some Issues

SET-UP and HOLD time, metastability



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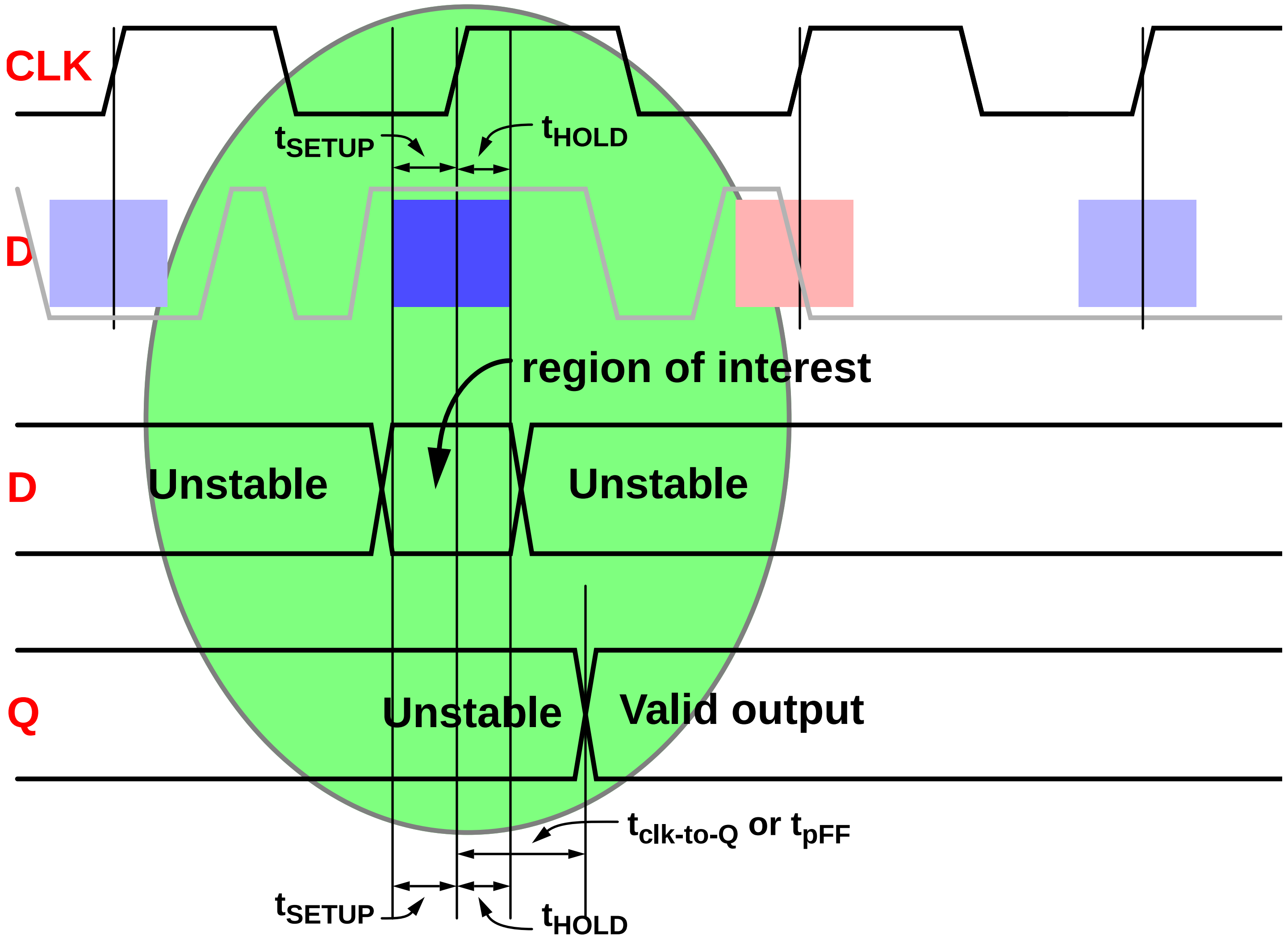
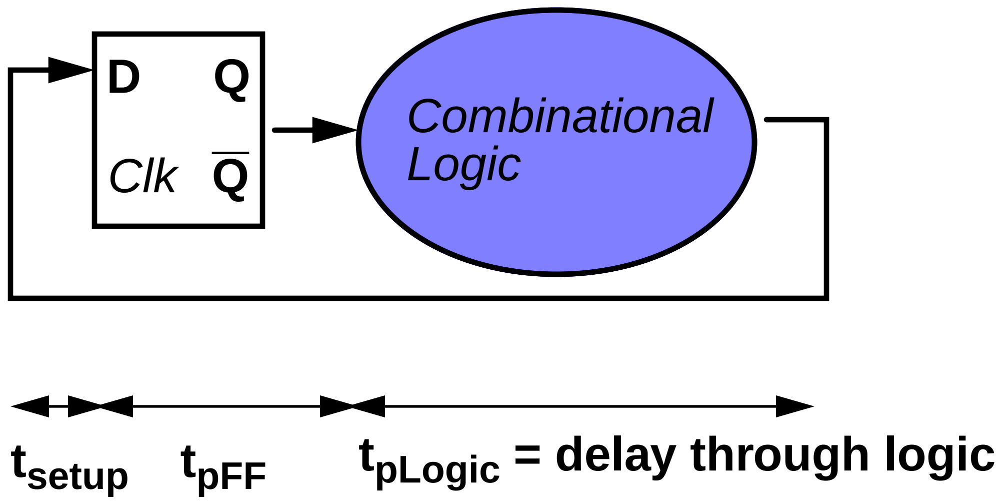
Some Issues

SET-UP and HOLD time, max. clock rate



Some Issues

SET-UP and HOLD time, max. clock rate



Max. clock frequency:

$$T_{min} \geq t_{pFF} + t_{pLogic} + t_{setup}$$

$$F_{max} \leq 1 / (t_{pFF} + t_{pLogic} + t_{setup})$$

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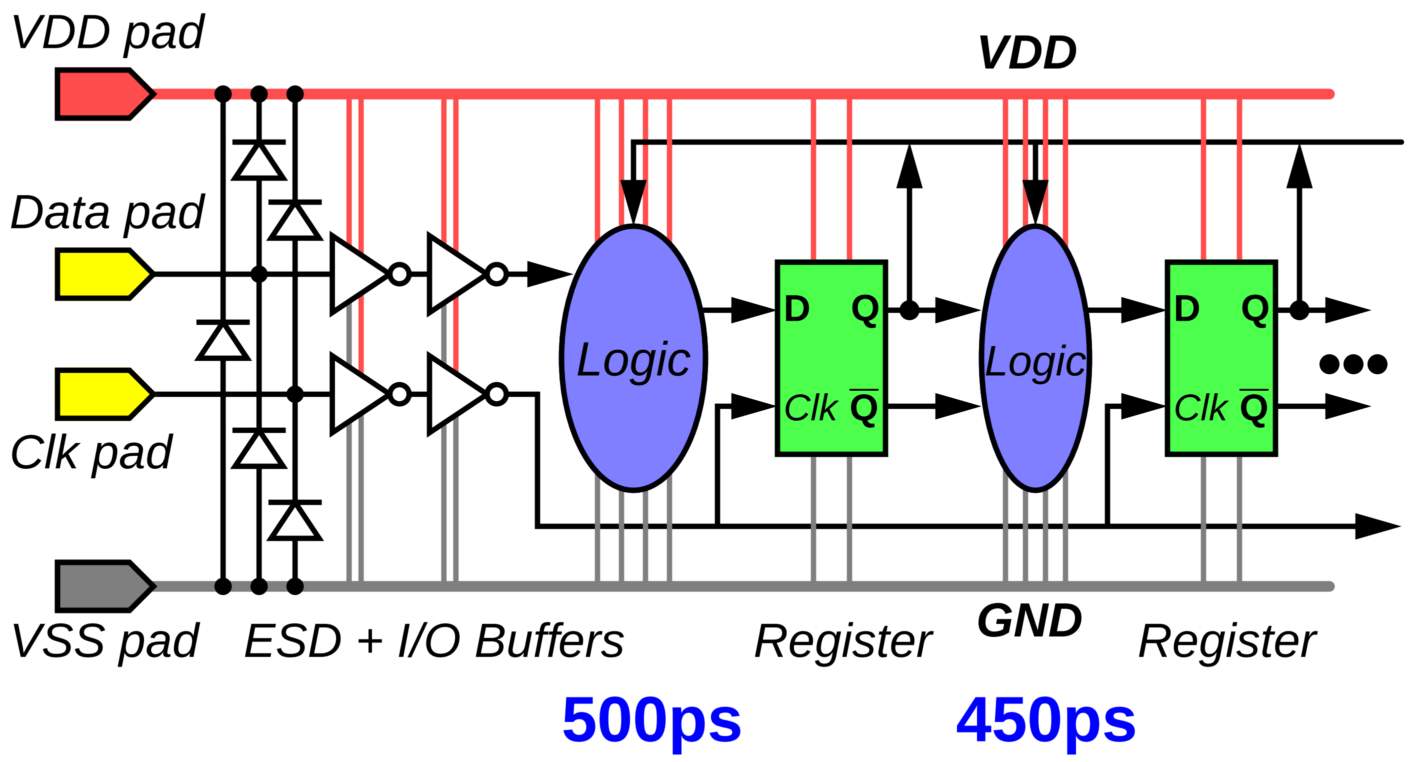
Pipelining

Goal: Increase max. clock rate



Worst-case logic delay: 950ps vs. 500ps

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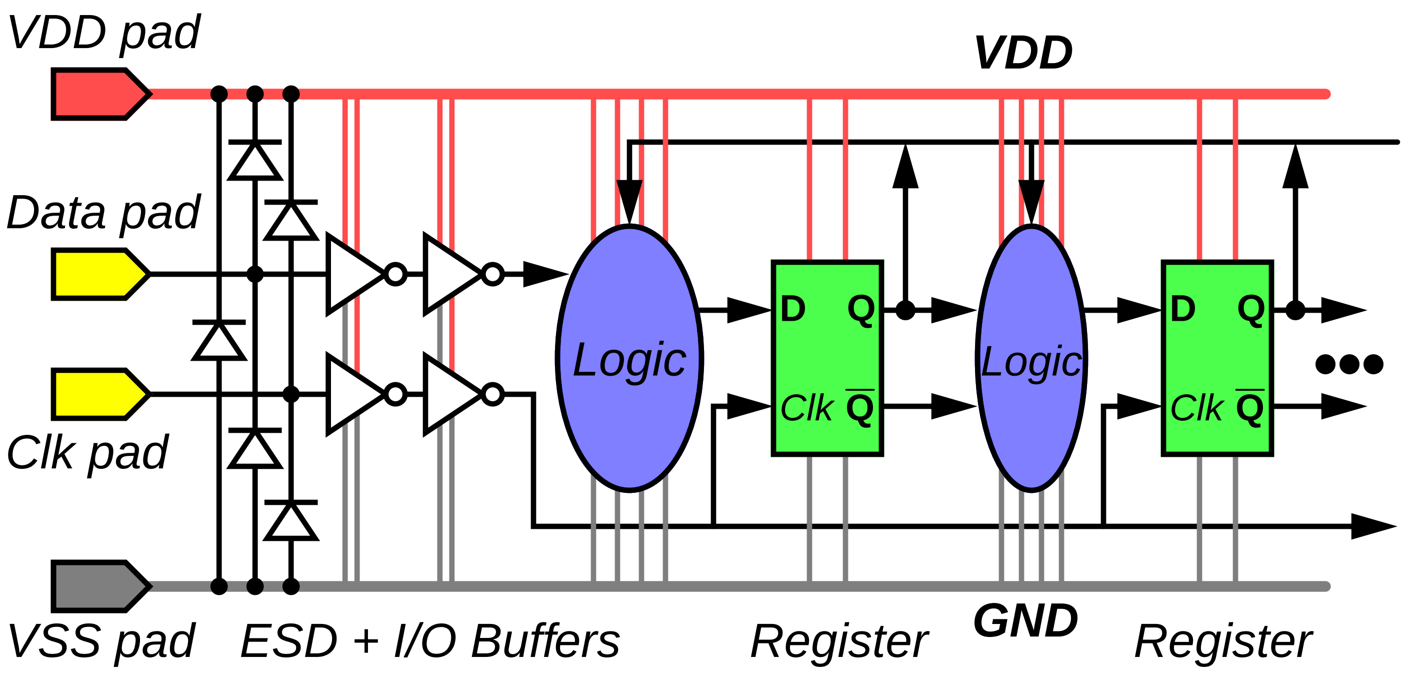
Pipelining

Goal: Decrease power dissipation



500ps, 100pF **450ps, 80pF**

Dynamic Power ~ CV^2*f*

- **Can reduce V_{DD} & f_{MAX} and maintain throughput**