Credit where credit is due:
Slides contain original artwork (© Jacob 2004) as well as material taken liberally from Irwin & Vijay’s CSE477 slides (PSU), Schmit & Strojwas’s 18-322 slides (CMU), Dally’s EE273 slides (Stanford), Wolf’s slides for Modern VLSI Design, and/or Rabaey’s slides (UCB).
Overview

- Wires and their physical properties (MOSFETs, too ...)
- LC/RC/RLC transmission lines, characteristic impedance, reflections
- Dynamic considerations (e.g. skin effect)
- The Bottom Line: propagation delay, transistor sizing, inductive (Ldi/dt) noise, capacitive coupling, signal degradation, various rules of thumb for design
Metal Layers in ICs

IBM’s 6-layer copper interconnect
Some Transmission Lines

- **Coaxial Cable**
  - Insulating jacket
  - Outer shield
  - Inner dielectric
  - Inner conductor

- **Twisted Pair**
  - Dielectric
  - Conductor

- **Microstrip**
  - Conductor
  - Dielectric
  - Gnd

- **Stripline**
  - Conductor
  - Dielectric
  - Gnd
Cross Section of PCB Board

- FR4 Dielectric
- M1 (signal layer)
- M2 (Ground plane)
- M3 (Power plane)
- M4 (signal layer)
- M5 (Power plane)
- M6 (signal layer)
Wires in Digital Systems

Physically, wires are

- Stripguides on (and in) printed circuit-board cards, layed over & sandwiched between groundplanes
- Stripguides on ICs, layered atop each other
- Conductors in cables & cable assemblies
- Connectors

We tend to treat them as IDEAL wires

- No delay (equipotential)
- No capacitance, inductance, or resistance

They are NOT ideal …

To build reliable systems, must understand properties & behavior
Metal Layers in ICs

Remember the $RC$ Constant $\tau$?
Metal Layers & Capacitances

- On-chip wires run in multiple layers with no explicit return planes (ground is used as implicit return)
- Thus, almost all capacitance of on-chip wire is to other wires (same plane, different plane, etc.)
- Capacitance of MOSFET scales with Vdd
Metal Layers & Resistances

- Resistance of conductor proportional to length/width, depends on material (resistivity), causes delay & loss
- Resistance of wire scales with square root of signaling frequency (at high speeds) ("skin effect")
- Process scaling tends to increase resistance
Wire Resistance

- \[ R = \frac{\rho l}{A} = \frac{\rho l}{(wh)} \] for rectangular wires (on-chip wires & vias, PCB traces)
- \[ R = \frac{\rho l}{A} = \frac{\rho l}{(\pi r^2)} \] for circular wires (off-chip, off-PCB)

<table>
<thead>
<tr>
<th>Material</th>
<th>Resistivity ( \rho ) (( \Omega )-m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silver (Ag)</td>
<td>1.6 x 10^{-8}</td>
</tr>
<tr>
<td>Copper (Cu)</td>
<td>1.7 x 10^{-8}</td>
</tr>
<tr>
<td>Gold (Au)</td>
<td>2.2 x 10^{-8}</td>
</tr>
<tr>
<td>Aluminum (Al)</td>
<td>2.7 x 10^{-8}</td>
</tr>
<tr>
<td>Tungsten (W)</td>
<td>5.5 x 10^{-8}</td>
</tr>
</tbody>
</table>
Sheet Resistance

\[ R = \frac{\rho l}{wh} = \frac{l}{w} \cdot \frac{\rho}{h} \] for rectangular wires

Sheet resistance \( R_{\text{sq}} = \frac{\rho}{h} \)

<table>
<thead>
<tr>
<th>Material</th>
<th>Sheet resistance ( R_{\text{sq}} ) (Ω/sq)</th>
</tr>
</thead>
<tbody>
<tr>
<td>n, p well diffusion</td>
<td>1000 to 1500</td>
</tr>
<tr>
<td>n+, p+ diffusion</td>
<td>50 to 150</td>
</tr>
<tr>
<td>polysilicon</td>
<td>150 to 200</td>
</tr>
<tr>
<td>polysilicon with silicide</td>
<td>4 to 5</td>
</tr>
<tr>
<td>Aluminum</td>
<td>0.05 to 0.1</td>
</tr>
</tbody>
</table>
Wire Capacitance

Common wire cross-sections/permittivities:

- Permittivity $\varepsilon = \varepsilon_0 \varepsilon_r$
- Permittivity of free space $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m

<table>
<thead>
<tr>
<th>Material</th>
<th>$\varepsilon_r$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Air</td>
<td>1</td>
</tr>
<tr>
<td>Teflon</td>
<td>2</td>
</tr>
<tr>
<td>Polymide</td>
<td>3</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>3.9</td>
</tr>
<tr>
<td>Glass-epoxy (PCB)</td>
<td>4</td>
</tr>
<tr>
<td>Alumina</td>
<td>10</td>
</tr>
<tr>
<td>Silicon</td>
<td>11.7</td>
</tr>
</tbody>
</table>
Inductance

When conductors of transmission line are surrounded by uniform dielectric, capacitance & inductance are related:

\[ CL = \varepsilon \mu \]

Inductive effects can be ignored

- if the resistance of the wire is substantial enough (as is the case for long Al wires with small cross section)
- if rise & fall times of applied signals are slow enough

So … inductance must be considered

- for off-chip signals (even power/ground)
- for future even-higher-speed on-chip signalling
MOSFET Resistance

Top view:

- MOS structure resistance - $R_{on}$
- Source and drain resistance
- Contact (via) resistance
- Wiring resistance
MOSFET Capacitance

Capacitances formed by p/n junctions

Depletion-region capacitances decrease with voltage across region; resistances increase with voltage across region
Wires & Models

Example Wires:

<table>
<thead>
<tr>
<th>Type</th>
<th>W</th>
<th>R</th>
<th>C</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-chip</td>
<td>0.6 μm</td>
<td>150k Ω/m</td>
<td>200 pf/m</td>
<td>600 nH/m</td>
</tr>
<tr>
<td>PC Board</td>
<td>150 μm</td>
<td>5 Ω/m</td>
<td>100 pf/m</td>
<td>300 nH/m</td>
</tr>
<tr>
<td>24AWG pair</td>
<td>511 μm</td>
<td>0.08 Ω/m</td>
<td>40 pf/m</td>
<td>400 nH/m</td>
</tr>
</tbody>
</table>

In a situation, use a *model* of wires that captures the properties we need:

- ideal, lumped L, R, or C
- LC, RC, RLC transmission line
- General LRCG transmission line

Appropriate choice of model depends on signaling frequency \( f_0 = \frac{R}{2\pi L} \)
General LRCG Model

Model an *infinitesimal* length of wire, $dx$, with lumped components $L$, $R$, $C$, and $G$ (inductance, resistance, capacitance, and conductance)

- **Drop across $R$ and $L$**
  \[
  \frac{\partial V}{\partial x} = RI + L\frac{\partial I}{\partial t}
  \]

- **Current into $C$ and $G$**
  \[
  \frac{\partial I}{\partial x} = GV + C\frac{\partial V}{\partial t}
  \]

- **Second-order differential equation**
  \[
  \frac{\partial^2 V}{\partial x^2} = RGV + (RC + LG)\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}
  \]

  For $G=0$:
  \[
  \frac{\partial^2 V}{\partial x^2} = RC\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}
  \]
Impedance

An infinite length of LRCG transmission line has impedance $Z_0$

Driving a line terminated into $Z_0$ is same as driving $Z_0$

In general, $Z_0$ is complex and frequency-dependent

For LC lines (operating at “high” frequencies), $Z_0$ is real-valued and independent of frequency

$typical$ $assumption: G = 0$
Cut-off Frequency $f_0$

$Z_0 = \left( \frac{R + j\omega L}{G + j\omega C} \right)^{1/2}$

- "Low" Freq: $R \gg j\omega L$
  
- Find $f_0$ where $R = j\omega L$
  
- $f_0 = \frac{R}{2\pi L}$

- "High" Freq: $R \ll j\omega L$

$Z_0 = \sqrt{\frac{R}{j\omega C}}$

$Z_0 = \sqrt{\frac{L}{C}}$

- Transmission lines have characteristic frequency $f_0$
- Below $f_0 \approx$ RC model, Above $f_0 \approx$ LC model
**Cut-off Frequency** $f_0$

**Example, 24AWG Pair**

- $f_0 = 33\text{kHz}$
- Below $f_0$, line is RC
- Above $f_0$, line is LC

\[ Z_0 = \left( \frac{0.08 + 400 \times 10^{-9} \times 2\pi f j}{40 \times 10^{-9} \times 2\pi f j} \right)^{\frac{1}{2}} \]
Cut-off Frequency $f_0$ II

L = 0.6 nH/mm
C = 73 nF/mm
$R_{dc} = 120\, \Omega /\text{mm}$
$f_0 = 32\, \text{GHz}$

L = 0.5 nH/mm
C = 104 fF/mm
$R_{dc} = 0.008\, \Omega /\text{mm}$
$f_0 = 2.5\, \text{MHz}$

~RC Model for on chip interconnects

~LC Model for PC Board traces

$Z_0 = \left(\frac{L}{C}\right)^{\frac{1}{2}} = \left(\frac{0.5\, \text{nH}}{0.1\, \text{pF}}\right)^{\frac{1}{2}} \approx 70\, \Omega$

1 mil = 0.001 inch

Example from Poulton 1999 ISSCC Tutorial
RC Lines (low frequency)

\[ \frac{\partial^2 V}{\partial x^2} = RGV + (RC + LG) \frac{\partial V}{\partial t} + LC \frac{\partial^2 V}{\partial t^2} \]

R >> jωL, governed by diffusion equation:

\[ \frac{\partial^2 V}{\partial x^2} = RC \frac{\partial V}{\partial t} \]

Signal diffuses down line, disperses:

R increases w/ length d
C increases with d
Delay & rise time both increase with RC, thus with d²

For a typical wire:
R = 150KΩ/m
C = 200pF/m
τ = RC = 30 μs/m²
= 30 ps/mm²
**LC Lines (high frequency)**

\[ \frac{\partial^2 V}{\partial x^2} = RGV + (RC + LG) \frac{\partial V}{\partial t} + LC \frac{\partial^2 V}{\partial t^2} \]

\( R \ll j\omega L \), governed by wave equation:

\[ \frac{\partial^2 V}{\partial x^2} = LC \frac{\partial^2 V}{\partial t^2} \quad V_i(x, t) = \left( \frac{Z_0}{Z_0 + R_S} \right) V_S \left( t - \frac{x}{v} \right) \]

Waveform on line is superposition of forward- and reverse-traveling waves:

- Waves travel with velocity \( v = (LC)^{-1/2} \)
- What happens when the wave gets to the end of line?
RLC/G Lines (general case)

\[ \frac{\partial^2 V}{\partial x^2} = RGV + (RC + LG) \frac{\partial V}{\partial t} + LC \frac{\partial^2 V}{\partial t^2} \]

Ignoring G, wave propagation equation:

\[ \frac{\partial^2 V}{\partial x^2} = RC \frac{\partial V}{\partial t} + LC \frac{\partial^2 V}{\partial t^2} \]

Lossy transmission line, dispersive waves:

Substrate-doping-dependent dispersion of a picosecond-scale pulse in propagation of an on-chip transmission line
RC vs. RLC

Output response of inverter with step input:

In reality, we have a non-zero inductance in series with the RC circuit. (Inductors and capacitors both “have memory”)

![Diagram of inverter with inductors and capacitors](image-url)
**RC vs. RLC**

Output response of inverter with step input:

- **RC Model**
- **RLC Model**

Result: slower response time, ringing
Impedance and Reflections

Terminating a Transmission Line:

\[ V_i \rightarrow Z_0 \rightarrow I_f \rightarrow \rightarrow I_r \rightarrow Z_T \rightarrow I_T \]

Telegrapher’s Equations:

\[ k_r = \frac{I_r}{I_i} = \frac{V_r}{V_i} = \frac{Z_T - Z_0}{Z_T + Z_0} \]

Reflection coefficient \( k_r \) may be complex for complex impedances \( Z_T \) — i.e., the reflected wave may be phase-shifted from the incident wave.

For real-valued \( Z_T \) the reflection coefficient is real, and the phase shift is either 0 (\( k_r \) positive) or \( \pi \) (\( k_r \) negative).
Impedance and Reflections

\[ k_r = \frac{I_r}{I_i} = \frac{V_r}{V_i} = \frac{Z_T - Z_0}{Z_T + Z_0} \]

**Matched Termination,** \( k_r = 0 \)

**Open-Circuit Termination,** \( k_r = 1 \)

**Short-Circuit Termination,** \( k_r = -1 \)
Impedance and Reflections

\[ 1V \quad 400\Omega \quad S \quad 50\Omega, 5\text{ns} \quad R \quad 1K\Omega \]
Impedance and Reflections

Values are typical for 8-mA CMOS driver with 1kΩ pullup
Impedance and Reflections

<table>
<thead>
<tr>
<th>Vwave</th>
<th>Vline</th>
<th>time t</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vi1</td>
<td>0.111</td>
<td>0.111</td>
</tr>
<tr>
<td>Vr1</td>
<td>0.101</td>
<td>0.212</td>
</tr>
<tr>
<td>Vi2</td>
<td>0.078</td>
<td>0.290</td>
</tr>
<tr>
<td>Vr2</td>
<td>0.071</td>
<td>0.361</td>
</tr>
<tr>
<td>Vi3</td>
<td>0.055</td>
<td>0.416</td>
</tr>
<tr>
<td>Vr3</td>
<td>0.050</td>
<td>0.465</td>
</tr>
<tr>
<td>Vi4</td>
<td>0.039</td>
<td>0.504</td>
</tr>
<tr>
<td>Vr4</td>
<td>0.035</td>
<td>0.539</td>
</tr>
<tr>
<td>Vi5</td>
<td>0.027</td>
<td>0.566</td>
</tr>
</tbody>
</table>
Impedance and Reflections

\[ \begin{align*}
V_{\text{line}}(t) & = V_S(t) + V_R(t) \\
& = V_S(t) + \frac{50 \Omega}{1000 \Omega} \cdot 50 \Omega \cdot 5 \text{ns} \\
& = V_S(t) + \frac{1}{20} \cdot 50 \Omega \cdot 5 \text{ns}
\end{align*} \]
Reflections, $Z_S < Z_0$

$$V_S = V_I \frac{Z_S}{Z_S + Z_0} = 2 \times \frac{50}{25 + 50} = 1.3333 \text{ V}$$

$$k_r \text{ (load)} = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{\text{inf} - 50}{\text{inf} + 50} = 1$$

$$k_r \text{ (source)} = \frac{Z_S - Z_0}{Z_S + Z_0} = \frac{25 - 50}{25 + 50} = -0.3333$$

$Z_S = 25 \Omega$

$Z_0 = 50 \Omega$

$Z_L = \text{inf} \Omega$

$V_I = 0v \rightarrow 2v$
Reflections, $Z_S < Z_0$

$$k_r \text{ (load)} = 1$$
$$k_r \text{ (source)} = -0.3333$$

$V_S$  $Z_0$  $V_L$

$V_I$  $Z_S$

$T_D = 250 \text{ ps}$

Time (ps)

0  250  500  750  1000

$V_S$

0  1.33 $V$  2.22 $V$  1.92 $V$

$V_L$

0  1.33 $V$  1.77 $V$  1.92 $V$  2.22 $V$  2.66 $V$
Reflections, $Z_S < Z_0$

Volts

- $V_{load}$
- $V_{source}$

Time (ps)

0 250 500 750 1000 1250 1500 1750

0.5v 1.0v 1.5v 2.0v 2.5v

0 250 500 750 1000 1250 1500 1750

UNIVERSITY OF MARYLAND
Add In Capacitance …

What if we throw in a capacitor (i.e., reality?)
Simple case: matched impedance at source end

[Diagram showing a circuit with a 1V source, a 50Ω resistor, and a 50Ω, 5ns transmission line, with receiving and source ends labeled.]
Impedance and Reflections

Modern systems have MANY, MANY, MANY potential sources of impedance-mismatch and/or reflections
Skin Effect

- At low frequencies, most of conductor’s cross-section carries current.
- As frequency increases, current moves to skin of conductor, back-EMF induces counter-current in body of conductor. Result: increased resistance, longer transmission delays.
- Skin effect most important at gigahertz frequencies.
Propagation Delay

Waves travel with velocity through medium:

\[ v = (LC)^{-1/2} = (\varepsilon_{di} \mu_{di})^{-1/2} = c_0(\varepsilon_r \mu_r)^{-1/2} \]

- \( \varepsilon \) is the permittivity of dielectric
- \( \mu \) is the permeability of dielectric

Relative permittivity \( \varepsilon_r \) and propagation speed (\( \mu_r \) is typically 1 for most dielectrics):

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>( \varepsilon_r )</th>
<th>Speed (cm/ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vacuum</td>
<td>1</td>
<td>30</td>
</tr>
<tr>
<td>SiO\textsubscript{2}</td>
<td>3.9</td>
<td>15</td>
</tr>
<tr>
<td>PC Board (epoxy glass)</td>
<td>5.0</td>
<td>13</td>
</tr>
<tr>
<td>Alumina (ceramic package)</td>
<td>9.5</td>
<td>10</td>
</tr>
</tbody>
</table>
Propagation Delay

But it’s not that simple ...

\[ \frac{R_{C_{polysilicon}}}{R_{C_{metal}}} \approx 20 \]

Metal Interconnect

Polysilicon Interconnect

\( V_{out} \)

TIME
Propagation Delay

Once again, $\tau = RC$

\[ C_{\text{wire}} = C_{\text{pp}} + C_{\text{fringe}} + C_{\text{interwire}} \]
\[ = \left( \frac{\varepsilon_{\text{di}}}{t_{\text{di}}} \right) WL \]
\[ + \left( \frac{2\pi\varepsilon_{\text{di}}}{\log(t_{\text{di}}/H)} \right) \]
\[ + \left( \frac{\varepsilon_{\text{di}}}{t_{\text{di}}} \right) HL \]
Propagation Delay

(from [Bakoglu89])
Insights

• For W/H < 1.5, the fringe component dominates the parallel-plate component. Fringing capacitance can increase overall capacitance by a factor of 10 or more.
• When W < 1.75H interwire capacitance starts to dominate
• Interwire capacitance is more pronounced for wires in the higher interconnect layers (further from the substrate)
• Wire delay nearly proportional to $L^2$

Rules of thumb:

• Never run wires in diffusion
• Use poly only for short runs
• Shorter wires – lower R and C
• Thinner wires – lower C but higher R
Wire Spacing

Intel P856.5
Al, 0.25µm

- Ω - 0.05
- Ω - 0.12
- Ω - 0.33
- Ω - 0.33
- Ω - 1.11

Scale: 2,160 nm

Intel P858
Al, 0.18µm

- Ω - 0.07
- Ω - 0.08
- Ω - 0.17
- Ω - 0.49
- Ω - 0.49

IBM CMOS-8S
CU, 0.18µm

- Ω - 0.05
- Ω - 0.10
- Ω - 0.10
- Ω - 0.49
- Ω - 0.49

from MPR 2000
Overcoming Interconnect $R$

Selective technology scaling
(scale $W$ while holding $H$ constant)

Use better interconnect materials

- lower resistivity materials like copper

As processes shrink, wires get shorter (reducing $C$) but they get closer together (increasing $C$) and narrower (increasing $R$). So RC wire delay increases and capacitive coupling gets worse.

Copper has about 40% lower resistivity than aluminum, so copper wires can be thinner (reducing $C$) without increasing $R$

- use silicides (WSi2, TiSi2, PtSi2 and TaSi)

Conductivity is 8-10 times better than poly alone

Use more interconnect layers

reduces the average wire length $L$, but beware of extra contacts
Inductive Noise

L di/dt noise (ground bounce):

Current flow changes direction when input (thus output) values change

Magnitude of current change is di
The time to switch directions is dt
The voltage-drop induced on this wire at time of switching is L di/dt
Inductive Noise

$L \frac{di}{dt}$ noise (ground bounce):

\[ \Delta V = L \frac{di}{dt} = \text{voltage-drop induced on this wire} \]

What comes out here?

Another inverter, elsewhere.

I/O Driver: