ENEE 359a

Digital VLSI Design

CMOS Memories and Systems: Part I, DRAM Systems

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Credit where credit is due:
Overview

DRAM:
- DRAM systems
- DRAM circuits

SRAM:
- SRAM systems
- SRAM circuits
- Register files
DRAM

Diagram showing the components of a DRAM cell:

- Switching element (transistor)
- Storage element (capacitor)
- Word Line
- Bit Line

Dual In-line Memory Module (DIMM)
(printed circuit board w/ DRAM chips on it)
The Memory System

... and DRAM’s place within it.

(typical PC-style desktop system)
DRAM-System Closeup

Traditional “JEDEC-Style” DRAM system
Memory Request Overview

**Steps not required for some processor/system controllers. protocol-dependent.**
Access-Protocol Basics

DRAM ORGANIZATION

- Bit Lines
- Word Lines
- Storage element (capacitor)
- Switching element
- Data In/Out Buffers
- Sense Amps
- Column Decoder
- Memory Array
- Row Decoder
- ... Bit Lines...
Access-Protocol Basics

BUS TRANSMISSION

CPU

MEMORY CONTROLLER

BUS

DRAM

Column Decoder

Sense Amps

... Bit Lines...

Row Decoder

... Word Lines...

Memory Array

Data In/Out Buffers
Access-Protocol Basics

[PRECHARGE and] ROW ACCESS

AKA: OPEN a DRAM Page/Row
or
ACT (Activate a DRAM Page/Row)
or
RAS (Row Address Strobe)
Access-Protocol Basics

COLUMN ACCESS

READ Command or
CAS: Column Address Strobe
Access-Protocol Basics

DATA TRANSFER

note: page mode enables overlap with CAS
Access-Protocol Basics

BUS TRANSMISSION

CPU

MEMORY CONTROLLER

BUS

DRAM

Column Decoder

Sense Amps

... Bit Lines...

Row Decoder

... Word Lines...

Memory Array

Data In/Out Buffers
Access-Protocol Basics

A: Transaction request may be delayed in Queue
B: Transaction request sent to Memory Controller
C: Transaction converted to Command Sequences (may be queued)

D: Command/s Sent to DRAM
E₁: Requires only a CAS or
E₂: Requires RAS + CAS or
E₃: Requires PRE + RAS + CAS
F: Transaction sent back to CPU

“DRAM Latency” = A + B + C + D + E + F
Access-Protocol Basics

Read Timing for Conventional DRAM

[Diagram showing the timing for read operations in DRAM, with RAS and CAS signals, and data transfer stages marked with Row Access, Column Access, and Data Transfer]
Access-Protocol Basics

Read Timing for Synchronous DRAM

(RAS + CAS + OE ... == Command Bus)
DRAM Circuit Basics

“Row” Defined

Row Size: 8 Kb @ 256 Mb SDRAM node
4 Kb @ 256 Mb RDRAM node
DRAM Circuit Basics

Sense Amplifier I: 6 rows shown

Sense and Amplify
DRAM Circuit Basics

Sense Amplifier I: 6 rows shown

V_{cc} (logic 1)  Gnd (logic 0)
DRAM Circuit Basics

Sense Amplifier II: Precharged

- Precharged to $V_{cc}/2$
- Sense and Amplify

$V_{cc}$ (logic 1)  Gnd (logic 0)  $V_{cc}/2$
DRAM Circuit Basics

Sense Amplifier III: Destructive Read

- $V_{cc}$ (logic 1)
- Gnd (logic 0)
- $V_{cc}/2$

Steps:
1. Sense and Amplify
2. Wordline Driven
DRAM Circuit Basics

“Column” Defined

Column: Smallest addressable quantity of DRAM on chip

SDRAM*: column size == chip data bus width (4, 8, 16, 32)
RDRAM: column size != chip data bus width (128 bit fixed)

SDRAM*: get n columns per access. n = (1, 2, 4, 8)
RDRAM: get 1 column per access.

* SDRAM means SDRAM and variants. i.e. DDR SDRAM
DRAM Architecture Basics

PHYSICAL ORGANIZATION

This is per bank ...
Typical DRAMs have 2+ banks
DRAM “Speed” Part I

How fast can I move data from DRAM cell to sense amp?

- **RCD** (Row Command Delay)
How fast can I get data out of sense amps back into memory controller?

$t_{CAS}$ aka $t_{CASL}$ aka $t_{CL}$

CAS: Column Address Strobe
CASL: Column Address Strobe Latency
CL: Column Address Strobe Latency
DRAM “Speed” Part III

How fast can I move data from DRAM cell into memory controller?

$t_{RAC} = t_{RCD} + t_{CAS}$

RAC (Random Access Delay)
DRAM “Speed” Part IV

How fast can I precharge DRAM array so I can engage another RAS?

$\begin{align*}
t_{RP} & \end{align*}$

RP (Row Precharge Delay)
DRAM “Speed” Part V

How fast can I read data from two different rows?

\[ t_{RC} = t_{RAS} + t_{RP} \]

RC (Row Cycle Time)
DRAM “Speed” Summary I

What do I care about?

- $t_{RCD}$
- $t_{CAS}$
- $t_{RP}$
- $t_{RC} = t_{RAS} + t_{RP}$
- $t_{RAC} = t_{RCD} + t_{CAS}$

**Seen in ads.**
Easy to explain
Easy to sell

**Embedded systems designers**

**DRAM manufacturers**

**Computer Architect:**
Latency bound code
i.e. linked list traversal

**RAS**: Row Address Strobe
**CAS**: Column Address Strobe
**RCD**: Row Command Delay
**RAC**: Random Access Delay
**RP**: Row Precharge Delay
**RC**: Row Cycle Time
### DRAM “Speed” Summary II

<table>
<thead>
<tr>
<th>DRAM Type</th>
<th>Frequency</th>
<th>Data Bus Width (per chip)</th>
<th>Peak Data Bandwidth (per Chip)</th>
<th>Random Access Time ($t_{\text{RAC}}$)</th>
<th>Row Cycle Time ($t_{\text{RC}}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC133 SDRAM</td>
<td>133</td>
<td>16</td>
<td>200 MB/s</td>
<td>45 ns</td>
<td>60 ns</td>
</tr>
<tr>
<td>DDR 266</td>
<td>133 * 2</td>
<td>16</td>
<td>532 MB/s</td>
<td>45 ns</td>
<td>60 ns</td>
</tr>
<tr>
<td>PC800 RDRAM</td>
<td>400 * 2</td>
<td>16</td>
<td>1.6 GB/s</td>
<td>60 ns</td>
<td>70 ns</td>
</tr>
<tr>
<td>FCRAM</td>
<td>200 * 2</td>
<td>16</td>
<td>0.8 GB/s</td>
<td>25 ns</td>
<td>25 ns</td>
</tr>
<tr>
<td>RLDRAM</td>
<td>300 * 2</td>
<td>32</td>
<td>2.4 GB/s</td>
<td>25 ns</td>
<td>25 ns</td>
</tr>
</tbody>
</table>

Data: Dec. 2002

DRAM is “slow”
But doesn’t have to be
$t_{\text{RC}} < 10\text{ns}$ achievable

Higher die cost → Not adopted in standard

Not commodity → Expensive
Signal Propagation

Ideal Transmission Line

\[ \sim 0.66c = 20 \text{ cm/ns} \]

PC Board + Module Connectors + Varying Electrical Loads

= Rather non-Ideal Transmission Line
DRAM Interface: Protocol

The Digital Fantasy

Pretend that the world looks like this

But...
**DRAM Interface: Signals**

*FCRAM side*
- VDDQ(Pad)
- DQ0-15 (Pin)
- DQS (Pin)
- VSSQ(Pad)

*Controller side*
- DQ0-15 (Pin)
- DQS (Pin)
- skew=158psec
- skew=102psec

*Toshiba Presentation, Denali MemCon 2002*
Interface: Clocking Issues

Figure 1: Sliding Time

What Kind of Clocking System?

Figure 2: H Tree?
Path Length Differential

Controller

Path #1

Path #2

A

Path #3

B

Bus Signal 2

Bus Signal 1

Intermodule Connectors

High Frequency AND Wide Parallel Busses are Difficult to Implement
Timing Variations

How many DIMMs in System?
How many devices on each DIMM?
Who built the memory module?

Infinite variations on timing!
Topology

DRAM System Topology Determines Electrical Loading Conditions and Signal Propagation Lengths
SDRAM Topology Example

Loading Imbalance
SDRAM Topology Example II

(Same topology, different drawing, a little more detail)
RDRAM Topology Example

Packets traveling down Parallel Paths. Skew is minimal by design.
I/O - Differential Pair

Single Ended Transmission Line

Differential Pair Transmission Line

Increase Rate of bits/s/pin?
Cost Per Pin?
Pin Count?
I/O - Multi Level Logic

Increase Rate of bits/s/pin
Packaging

- **DIP**
  - "good old days"

- **SOJ**
  - Small Outline J-leads

- **TSOP**
  - Thin Small Outline Package

- **LQFP**
  - Low Profile Quad Flat Package

<table>
<thead>
<tr>
<th>Features</th>
<th>Target Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>FBGA</td>
</tr>
<tr>
<td></td>
<td>LQFP</td>
</tr>
<tr>
<td>Speed</td>
<td>800MBps</td>
</tr>
<tr>
<td></td>
<td>550Mbps</td>
</tr>
<tr>
<td>Vdd/Vddq</td>
<td>2.5V/2.5V (1.8V)</td>
</tr>
<tr>
<td>Interface</td>
<td>SSTL_2</td>
</tr>
<tr>
<td>Row Cycle Time</td>
<td>35ns</td>
</tr>
</tbody>
</table>

Memory Roadmap for Hynix NetDDR II
Access Protocol

Single Cycle Command

Multiple Cycle Command
Access Protocol (r/r)

Consecutive Cache Line Read Requests to Same DRAM Row

a = Active (open page)
r = Read (Column Read)
d = Data (Data chunk)
Access Protocol (r/w)

Case 1: Read Following a Write Command to Different DRAM Devices

Case 2: Read Following a Write Command to Same DRAM Device

Soln: Delay Data of Write Command to match Read Latency
Address Mapping

Physical Address

Device Id
Row Addr
Col Addr
Bank Id

Access Distribution for Temp Control
Avoid Bank Conflicts
Access Reordering for performance
Example: Bank Conflicts

Multiple Banks to Reduce Access Conflicts

Read 05AE5700 → Device id 3, Row id 266, Bank id 0
Read 023BB880 → Device id 3, Row id 1BA, Bank id 0
Read 05AE5780 → Device id 3, Row id 266, Bank id 0
Read 00CBA2C0 → Device id 3, Row id 052, Bank id 1

More Banks per Chip == Performance == Logic Overhead
Example: Access Reordering

1. Read 05AE5700 → Device id 3, Row id 266, Bank id 0
2. Read 023BB880 → Device id 3, Row id 1BA, Bank id 0
3. Read 05AE5780 → Device id 3, Row id 266, Bank id 0
4. Read 00CBA2C0 → Device id 1, Row id 052, Bank id 1

Act = Activate Page (Data moved from DRAM cells to row buffer)
Read = Read Data (Data moved from row buffer to memory controller)
Prec = Precharge (close page/evict data in row buffer/sense amp)
## Technology Roadmap (ITRS)

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Semi Generation (nm)</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
</tr>
<tr>
<td>CPU MHz</td>
<td>3990</td>
<td>6740</td>
<td>12000</td>
<td>19000</td>
<td>29000</td>
</tr>
<tr>
<td>MLogicTransistors/cm^2</td>
<td>77.2</td>
<td>154.3</td>
<td>309</td>
<td>617</td>
<td>1235</td>
</tr>
<tr>
<td>High Perf chip pin count</td>
<td>2263</td>
<td>3012</td>
<td>4009</td>
<td>5335</td>
<td>7100</td>
</tr>
<tr>
<td>High Performance chip cost (cents/pin)</td>
<td>1.88</td>
<td>1.61</td>
<td>1.68</td>
<td>1.44</td>
<td>1.22</td>
</tr>
<tr>
<td>Memory pin cost (cents/pin)</td>
<td>0.34 - 1.39</td>
<td>0.27 - 0.84</td>
<td>0.22 - 0.34</td>
<td>0.19 - 0.39</td>
<td>0.19 - 0.33</td>
</tr>
<tr>
<td>Memory pin count</td>
<td>48-160</td>
<td>48-160</td>
<td>62-208</td>
<td>81-270</td>
<td>105-351</td>
</tr>
</tbody>
</table>

**Trend:** Free Transistors & Costly Interconnects
Choices for Future

- **Direct Connect**
  - Custom DRAM: Highest Bandwidth + Low Latency

- **Indirect Connection**
  - Inexpensive DRAM: Highest Bandwidth + Highest Latency

- **Commodity DRAM**
  - Low Bandwidth + Low/Moderate Latency

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**SLIDE 50**
DRAM Evolutionary Tree

Conventional DRAM

(Mostly) Structural Modifications Targeting Throughput

FPM → EDO → P/BEDO → SDRAM

Structural Modifications Targeting Latency

MOSYS

FCRAM

VCDRAM

Interface Modifications Targeting Throughput

ESDRAM

Rambus, DDR/2

Future Trends
DRAM Evolution

Read Timing for Conventional DRAM

- Row Access
- Column Access
- Transfer Overlap
- Data Transfer
DRAM Evolution

Read Timing for Fast Page Mode

- Row Access
- Column Access
- Transfer Overlap
- Data Transfer
DRAM Evolution

Read Timing for Extended Data Out

- Row Access
- Column Access
- Transfer Overlap
- Data Transfer

Diagram showing RAS, CAS, Address, and DQ with timeline for data transfer and overlap.
DRAM Evolution

Read Timing for Burst EDO

- Row Access
- Column Access
- Transfer Overlap
- Data Transfer

RAS

CAS

Address

Column Address

Row Address

DQ

Valid Data

Valid Data

Valid Data

Valid Data
DRAM Evolution

Read Timing for Pipeline Burst EDO

- RAS (Row Address Strobe)
- CAS (Column Address Strobe)
- DQ (Data Out)
- Timing Overlap

Row Access
Column Access
Transfer Overlap
Data Transfer
DRAM Evolution

Read Timing for Synchronous DRAM

(RAS + CAS + OE ... == Command Bus)
DRAM Evolution

Inter-Row Read Timing for ESDRAM

Regular CAS-2 SDRAM, R/R to same bank

ESDRAM, R/R to same bank
DRAM Evolution

Write-Around in ESDRAM

Regular CAS-2 SDRAM, R/W/R to same bank, rows 0/1/0

ESDRAM, R/W/R to same bank, rows 0/1/0

(can second READ be this aggressive?)
Segment cache is software-managed, reduces energy
DRAM Evolution

Internal Structure of Fast Cycle RAM

SDRAM

8M Array (8Kr x 1Kb)

Sense Amps

Row Decoder

13 bits

t\text{RCD} = 15\text{ns}
(two clocks)

FCRAM

8M Array (?)

Sense Amps

Row Decoder

15 bits

t\text{RCD} = 5\text{ns}
(one clock)

Reduces access time and energy/access
DRAM Evolution

Internal Structure of MoSys 1T-SRAM