1. **Flip-Flop Timing**

In the flip-flop below, the gates are annotated with their delay in time units. Assume the initial state of the flip-flop is $Q = 1$, $\bar{Q} = 0$.

A. Fill out the timing diagram to illustrate the behavior of the circuit.

B. Determine the worst-case Clock-to-$Q$ propagation time.

C. Determine the worst-case set-up (D-to-Clk) time.

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**Timing Diagram**

```
D  CLK
   #3   #1  x  #3  #2
    #3   #1  y  #3  #2

0  2  4  6  8  10  12  14  16  18  20  22  24  26  28  30
```

```
D

CLK

x

y

Q

\bar{Q}
```
2. **Elmore Delay**

Using the Elmore-delay model, compute the RC delay from the source node (node 0) to sink nodes 1 through 5.