ENEE 302H
Digital Electronics

CMOS Memories and Systems: Part II, DRAM Circuits, SRAM

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Credit where credit is due:
Slides contain original artwork (© Jacob 1999–2004, Wang 2003/4) as well as material taken from Keeth & Baker’s DRAM Circuit Design.
Overview

DRAM:
- DRAM systems
- DRAM circuits

SRAM:
- SRAM systems
- SRAM circuits
- Register files
The Original 3T DRAM Cell

First generation DRAM cell

- MOSFET #2 is used as storage node (obvious to see why “dynamic”)
- Read columnline precharged for read; line either pulled to GND or not.
Second Generation 1T1C Cell

Digitline, columnline, or bitline

Wordline or rowline

- Wordline can be polysilicon; MOSFET formed by wordline over n+ active area
- To write full Vcc to storage capacitor, rowline (gate) must be driven to voltage \( V_{ccp} > Vcc + V_{th} \)
- Bitline can be metal or polysilicon
- Charge-sharing: what potential should be at other side of storage capacitor? (e.g. \( V_0 = 0, V_1 = Vcc \))
Wordline presents large capacitive load; slow, limits $t_{RC}$ (time to open & close row)

- Use wordline driver: large FETs (remember scaling?)
- Polysilicon wordline usually topped with silicide (“polycide” wordline); increases conductivity
- Additional drivers can be placed along length
- Wordline can be “stitched” with pieces of metal
- Typical organization: 512 wordlines x 512 bitlines
DRAM Array: Open Bitline

- Adjacent cells share connection to bitline
- Note change in orientation (rotated $90^\circ$)
Open Bitline Array & Cells

Wordline drivers

Sense Amps

Wordline drivers

Wordline

Bitline

Capacitor

Active area

Bitline contact
Folded Bitline Array & Cell

Routing BLX and BLX* together improves noise immunity (esp. in conjunction with bitline twisting ... )
Open vs. Folded Cell Areas

Open bitline cell:
1F x 3F = 6F^2

Folded bitline cell:
2F x 4F = 8F^2

Cell pitch (2 cells)
1/2 + 7 + 1/2 = 8F

Cell pitch
1/2 + 1 + 1 + 1/2 = 3F

Bitline pitch
2F
Sensing I

Recall behavior of nFET:

- Scenario 1: nFET conducts when gate voltage exceeds \( \min\{\text{Source, Drain}\} \) (GND) by \( V_{th} \)
- Scenario 2: nFET conducts when gate voltage exceeds \( \min\{\text{Source, Drain}\} \) (Vcc/2) by \( V_{th} \)

\[ V_X = \frac{V_b C_b + V_c C_c}{C_b + C_c} \]
Passing Logic 1:
- Capacitor begins to discharge when wordline exceeds bitline PRECHARGE voltage by $V_{th}$

Passing Logic 0:
- Capacitor begins to discharge when wordline exceeds $V_{th}$
**Sense Amplifiers I**

**Circuit diagram:**

- Initially, ACT at Vss (GND) and NLAT* held at Vcc/2 (both BL1 and BL1* are at Vcc/2 as well)
- **To read:** Wordline pulled to Vcc+Vth, BL1/* changes
- **To sense:** first, NLAT* is pulled towards ground
- Then ACT is pulled towards Vcc
Sense Amplifiers II

Basic idea:

![Sense Amplifier Diagram](image-url)
Sense Amplifiers III

![Diagram of sense amplifiers with labels for BL1, BL1*, ACT, and NLAT*]
Equilibration I

Textbook’s term: equalization
Equilibration II

![Circuit Diagram]

LAYOUT:
- poly
- n active area

BL1
VCC/2
BL1*
EQ
Bitline Twisting

... this is just a small sample
Cells: Buried Capacitor

- Bitline
- Interlayer dielectric
- ONO dielectric
- Poly3 cellplate
- Bitline contact
- Wordline
- Field poly
- n+ active
- n+ active
- p substrate
- Poly2 storage node
- FOX
Cells: Buried Bitline/Digitline

- Buried Bitline/Digitline
- Bitline
- Bitline contact
- Interlayer dielectric
- ONO dielectric
- Poly3 cellplate
- Wordline
- Poly2 storage node
- n+ active
- n+ active
- p substrate
- Field poly
- FOX
Cells: Trench Capacitor

- Bitline
- Bitline contact
- Wordline
- Poly strap
- Poly storage node
- ONO dielectric
- Heavily doped substrate region
- Field poly
- FOX
Cells: Buried Bitline/Digitline

- Bitline
- Bitline contact
- Interlayer dielectric
- ONO dielectric
- Poly3 cellplate
- n+ active
- FOX
- n+ storage node
- p substrate
- Wordline
- Poly2 storage node
Cells: Trench Capacitor

- Bitline
- Poly strap
- Bitline contact
- Wordline
- Poly storage node
- ONO dielectric
- Heavily doped substrate region
- Field poly
- FOX
- n+ active
- Poly strap
- Poly storage node
- ONO dielectric
- Heavily doped substrate region
- Field poly
- FOX
- n+ active
Cells: eDRAM (logic process)

Basic idea: replace funky capacitor structure (which requires special process technology to produce) with something that looks like logic.

DRAM is now “embedded” into a logic process: on same chip as CPU cores, etc.

Question: do we still tie far side to VCC/2?
Cells: eDRAM (logic process)

The components

Active
Polysilicon
Contact
Metal
Cells: eDRAM (logic process)

The cell
Cells: eDRAM (logic process)

- VDD
- WL
- BL
- i, i-1, i+1, i+2
Cells: eDRAM (logic process)

Why is poly plate held at (global) VDD?
eDRAM: 2-bit cell (CMU)

Active area
eDRAM: 2-bit cell (CMU)

Poly I
eDRAM: 2-bit cell (CMU)

Poly II
eDRAM: 2-bit cell (CMU)

Via & Metal 1
eDRAM: 2-bit cell (CMU)