1. **Flip-Flop Timing**

In the flip-flop below, the gates are annotated with their delay in time units. Assume the initial state of the flip-flop is \( Q = 1, \overline{Q} = 0 \).

A. Fill out the timing diagram to illustrate the behavior of the circuit.

B. Determine the worst-case Clock-to-Q propagation time.

C. Determine the worst-case set-up (D-to-Clk) time.
2. **Elmore Delay**

Using the Elmore-delay model, compute the RC delay from the source node (node 0) to sink nodes 1 through 5.