Homework 3

ENEE 302h: Digital Electronics, Fall 2004
Assigned: Mon, Oct 04 Due: Mon, Oct 11

1. Transistor Sizing

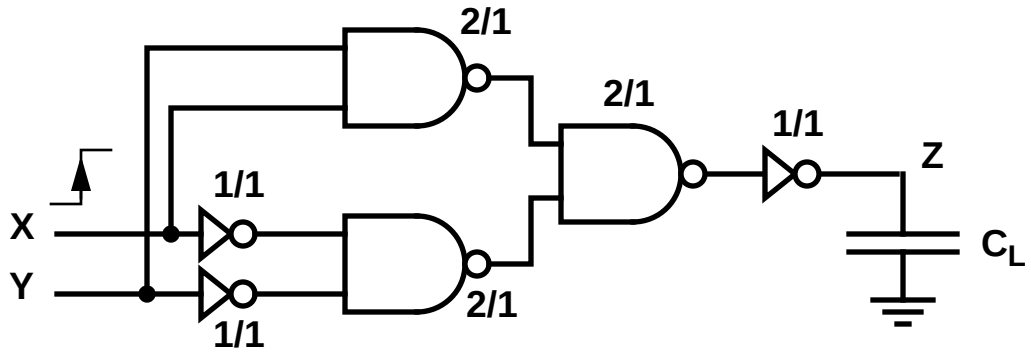
Consider a complex CMOS logic gate that implements the function Y = ~(ABC + DE + EFG).

A. Draw the transistor-level schematic of the gate (do not try to optimize it).

B. Size all NMOS and PMOS transistors such that the worst-case rise and fall delays are equal to the fall delay of a minimum-sized CMOS inverter (i.e., W/L for NMOS transistor = 1).

2. Circuit Delay

Consider the CMOS circuit shown below.



In the figure, the W/L ratios for each gate apply to *both* NMOS and PMOS transistors. We want to determine the delay from a rising transition ($0 \rightarrow 1$) on input X to the output Z. Let us denote by $\tau = R_nC_n$ the product of the effective on-resistance and gate capacitance of the minimum-sized NMOS transistor, i.e. $(W/L)_n = 1/1$. For the minimum-sized PMOS transistor, we have $R_p = 2R_n$. Also, the output Z drive load is $C_L = 10C_n$.

A. Assuming that the rise and fall times are good approximations of the propagation delay, determine the delay from X to Z, in terms of τ, when Y = 0.

B. Now, assume that Y = 1. What is the new value for the propagation delay from X to Z? Can you comment on this?