1. Transistor Switching

CMOS gate

2. \( T = R_C n \)

A

- transition in bottom NAND 0 to 1 \( t_{PHL} = 0.69 \times \frac{2R_m \times C_n}{2} = 0.69 \times R_mC_n \)
- no transition in top NAND stays 1
- transition in top NOT from 1 to 0 \( t_P = 0.69 \times R_mC_n \)
- no transition in bottom NOT
- last NAND 1 to 0 \( t_{PHL} = 0.69 \times \frac{R_m \times C_n}{2} = 0.345 \times R_mC_n \)
- last NOT 0 to 1 \( t_P = 0.69 \times R_mC_n = 0.69 \times R_mC_n \)

\[ \text{total} = R_mC_n \left( 0.69 + 0.345 + 0.69 + 0.69 \right) = 2.625 \times R_mC_n \]

B

- transition in top NAND from 1 to 0 \( t_{PHL} = 0.345 \times R_mC_n \)
- no change in bottom NAND, so we can ignore transition in top NOT
- last NAND 0 to 1 \( t_{PHL} = 0.69 \times \frac{2R_m \times C_n}{2} = 0.69 \times R_mC_n \)
- last NOT 1 to 0 \( t_P = 0.69 \times R_mC_n \)

\[ \text{total} = R_mC_n \left( 0.69 + 0.69 + 2 \times 0.69 \right) = 3.935 \times R_mC_n \]