CMOS Memories and Systems: Part II, DRAM Circuits, SRAM

Prof. Bruce Jacob
blj@eng.umd.edu

TA: Katie Baynes
ktbaynes@eng.umd.edu

Credit where credit is due:
Slides contain original artwork (© Jacob 1999–2004, Wang 2003/4) as well as material taken from Keeth & Baker’s DRAM Circuit Design.
Overview

DRAM:
- DRAM systems
- DRAM circuits

SRAM:
- SRAM systems
- SRAM circuits
- Register files
The Original 3T DRAM Cell

First generation DRAM cell

- MOSFET #2 is used as storage node (obvious to see why “dynamic”)
- Read columnline precharged for read; line either pulled to GND or not.
Second Generation 1T1C Cell

Digitline, columnline, or bitline

Wordline or rowline

\[ V_{cc}/2 \]

\[ V_{c} \]

\[ V_{b} \]

\[ V_{x} = \frac{V_{b}C_{b} + V_{c}C_{c}}{C_{b} + C_{c}} \]

- Wordline can be polysilicon; MOSFET formed by wordline over n+ active area
- To write full Vcc to storage capacitor, rowline (gate) must be driven to voltage \( V_{ccp} > V_{cc} + V_{th} \)
- Bitline can be metal or polysilicon
- Charge-sharing: what potential should be at other side of storage capacitor? (e.g. \( V_{0} = 0, V_{1} = V_{cc} \))
Wordline presents large capacitive load; slow, limits $t_{RC}$ (time to open & close row)

- Use wordline driver: large FETs (remember scaling?)
- Polysilicon wordline usually topped with silicide ("polycide" wordline); increases conductivity
- Additional drivers can be placed along length
- Wordline can be “stitched” with pieces of metal
- Typical organization: 512 wordlines x 512 bitlines
**DRAM Array: Open Bitline**

- Adjacent cells share connection to bitline
- Note change in orientation (rotated 90°)
Open Bitline Array & Cells

WL0 WL1 WL2 WL3 WLA WLB WLC WLD

Wordline drivers

BL3 BL3* BL2 BL2*

WL0 WL1 WL2 WL3

Wordline drivers

Sense Amps

BL1 BL1* BL0 BL0*

Wordline drivers

WL1 Wordline WL2 WL3 Bitline WL4 WL5

Capacitor

Active area

Bitline contact
Routing BLX and BLX* together improves noise immunity (esp. in conjunction with *bitline twisting ... *)
Open vs. Folded Cell Areas

Open bitline cell:
1F x 3F = 6F²

Folded bitline cell:
2F x 4F = 8F²

Cell pitch:
1/2 + 1 + 1 + 1/2 = 3F

Bitline pitch:
2F
Sensing I

Recall behavior of nFET:

- **Scenario 1**: nFET conducts when gate voltage exceeds \( \min\{\text{Source, Drain}\} \) (GND) by \( V_{\text{th}} \)
- **Scenario 2**: nFET conducts when gate voltage exceeds \( \min\{\text{Source, Drain}\} \) (Vcc/2) by \( V_{\text{th}} \)

\[
V_X = \frac{V_b C_b + V_c C_c}{C_b + C_c}
\]

- **Scenario 1**: nFET conducts when gate voltage exceeds \( \min\{\text{Source, Drain}\} \) (GND) by \( V_{\text{th}} \)
- **Scenario 2**: nFET conducts when gate voltage exceeds \( \min\{\text{Source, Drain}\} \) (Vcc/2) by \( V_{\text{th}} \)
### Sensing II

#### Passing Logic 1:
- Capacitor begins to discharge when wordline exceeds bitline PRECHARGE voltage by $V_{th}$

#### Passing Logic 0:
- Capacitor begins to discharge when wordline exceeds $V_{th}$

Mathematically:

$$V_x = \frac{V_b C_b + V_c C_c}{C_b + C_c}$$

$$V_{signal} = \frac{V_c C_c}{C_b + C_c}$$
Sense Amplifiers I

Circuit diagram:

- Initially, ACT at Vss (GND) and NLAT* held at Vcc/2 (both BL1 and BL1* are at Vcc/2 as well)
- **To read:** Wordline pulled to Vcc+Vth, BL1/* changes
- **To sense:** first, NLAT* is pulled towards ground
- Then ACT is pulled towards Vcc
Sense Amplifiers II

Basic idea:

\[ \text{NLAT}^* \rightarrow \text{ACT} \rightarrow \text{VCC} \rightarrow \text{GND} \rightarrow \text{OR} \rightarrow \text{BL1}^* \]

\[ \text{ACT} \rightarrow \text{VCC} \rightarrow \text{GND} \rightarrow \text{NLAT}^* \rightarrow \text{BL1}^* \]
Sense Amplifiers III

NLAT* ACT
BL1

V

Vccp

Vcc

Vcc/2

Wordline voltage

NLat*

ACT

BL1

BL1*

Vth

time
Equilibration I

Textbook’s term: *equalization*
Bitline Twisting

None

Single

Triple

Complex

… this is just a small sample
Cells: Buried Capacitor

Bitline

Interlayer dielectric

Bitline contact

ONO dielectric Poly3 cellplate

Wordline

p substrate

n+ active

n+ Poly2 storage node

n+

Field poly FOX
Cells: Buried Bitline/Digitline

- Bitline
- Bitline contact
- Interlayer dielectric
- ONO dielectric
- Poly3 cellplate
- Wordline
- p substrate
- n+ active
- n+ active
- n+ active
- n+ active
- Poly2 storage node
- Field poly
- FOX
Cells: Trench Capacitor

- Bitline
- Bitline contact
- Wordline
- Poly storage node
- ONO dielectric
- Heavily doped substrate region
- Poly strap
- n+ active
- Field poly
- FOX
- Poly strap
Cells: Buried Capacitor

Bitline

Interlayer dielectric

ONO dielectric

Poly3 cellplate

Bitline contact

n+ active

n+ active

Wordline

Poly2 storage node

p substrate

n+ active

Field poly

FOX
Cells: Buried Bitline/Digitline

- Bitline
- Bitline contact
- Interlayer dielectric
- ONO dielectric
- Poly3 cellplate
- Wordline
- n+ active
- n+ storage node
- p substrate
- Field poly
- FOX
- Poly2 storage node
Cells: Trench Capacitor

- Bitline
- Poly strap
- Bitline contact
- Wordline
- Field poly
- n+ active
- Poly storage node
- ONO dielectric
- Heavily doped substrate region

- Trench Capacitor components:
  - ONO dielectric
  - Heavily doped substrate region
  - Poly storage node
  - Field poly
  - Bitline
  - Poly strap
  - Bitline contact
  - Wordline

- Diagram shows the layout and components of a trench capacitor memory cell.
Cells: eDRAM (logic process)

- Basic idea: replace funky capacitor structure (which requires special process technology to produce) with something that looks like logic
- DRAM is now “embedded” into a logic process: on same chip as CPU cores, etc.
- Question: do we still tie far side to VCC/2?

Diagram:
- Bitline
- Wordline
- Sense amp
Cells: eDRAM (logic process)

The components

- Active
- Polysilicon
- Contact
- Metal
Cells: eDRAM (logic process)

The cell

WL  VDD

to Sense Amp

to sense amp
Cells: eDRAM (logic process)

- VDD
- WL
- BL

Diagram showing the layout of eDRAM cells with VDD, WL, and BL connections.
Cells: eDRAM (logic process)

Why is poly plate held at (global) VDD?
eDRAM: 2-bit cell (CMU)

Active area
eDRAM: 2-bit cell (CMU)
eDRAM: 2-bit cell (CMU)
eDRAM: 2-bit cell (CMU)

Via & Metal 1
eDRAM: 2-bit cell (CMU)