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Digital Electronics

CMOS Memories and Systems: Part I, DRAM Systems

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Credit where credit is due:
Overview

DRAM:
- DRAM systems
- DRAM circuits

SRAM:
- SRAM systems
- SRAM circuits
- Register files
Dual In-line Memory Module (DIMM)

(printed circuit board w/ DRAM chips on it)
The Memory System

... and DRAM’s place within it.

(typical PC-style desktop system)
DRAM-System Closeup

Traditional “JEDEC-Style” DRAM system
Memory Request Overview

![Memory Request Diagram]

- **Part A: Searching on-chip for data**
  - **Fetch**
  - **Decode**
  - **Exec**
  - **Mem**
  - **WB**

- **Part B: Going off-chip for data**
  - **BIU (Bus Interface Unit)**
  - **DTLB**
  - **L1 cache**
  - **L2 cache**

Stages of instruction execution:
- **virtual to physical address translation**
- **[A_1]** L1 D-Cache access. If miss then proceed to
- **[A_2]** L1 Cache access. If miss then send to BIU
- **[A_3]** L2 Cache access. If miss then send to BIU
- **Bus Interface Unit (BIU)** obtains data from main memory **[A_4 + B]**

**Steps not required for some processor/system controllers. protocol-dependent.**

**Progression of a Memory Read Transaction Request Through Memory System**
Access-Protocol Basics

DRAM ORGANIZATION

- Storage element (capacitor)
- Word Line
- Bit Line
- Switching element
- Data In/Out Buffers
- Sense Amps
- Column Decoder
- Memory Array
- Bit Lines
- Word Lines
Access-Protocol Basics

BUS TRANSMISSION

- CPU
- MEMORY CONTROLLER
- BUS TRANSMISSION
- DRAM
  - Column Decoder
  - Sense Amps
  - Memory Array
  - Row Decoder
  - ...Word Lines...
  - ...Bit Lines...
Access-Protocol Basics

[PRECHARGE and] ROW ACCESS

AKA: OPEN a DRAM Page/Row
or
ACT (Activate a DRAM Page/Row)
or
RAS (Row Address Strobe)
Access-Protocol Basics

COLUMN ACCESS

CPU

MEMORY CONTROLLER

BUS

DRAM

Row Decoder

...Word Lines...

Sense Amps

Data In/Out Buffers

Column Decoder

...Bit Lines...

Memories

READ Command

or

CAS: Column Address Strobe
Access-Protocol Basics

DATA TRANSFER

... with optional additional

**CAS**: Column Address Strobe

note: page mode enables overlap with CAS
Access-Protocol Basics

BUS TRANSMISSION

CPU

MEMORY CONTROLLER

BUS

DRAM

Column Decoder

Sense Amps

... Bit Lines...

Row Decoder

... Word Lines...

Memory Array

Data In/Out Buffers
Access-Protocol Basics

A: Transaction request may be delayed in Queue
B: Transaction request sent to Memory Controller
C: Transaction converted to Command Sequences (may be queued)

D: Command/s Sent to DRAM
E_1: Requires only a CAS or
E_2: Requires RAS + CAS or
E_3: Requires PRE + RAS + CAS

F: Transaction sent back to CPU

“DRAM Latency” = A + B + C + D + E + F
Access-Protocol Basics

Read Timing for Conventional DRAM

- RAS (Row Address Strobe)
- CAS (Column Address Strobe)
- DQ (Data Out)
- Valid Dataout
- Row Access
- Column Access
- Data Transfer
Access-Protocol Basics

Read Timing for Synchronous DRAM

(RAS + CAS + OE ... == Command Bus)
DRAM Circuit Basics

“Row” Defined

Row Size: 8 Kb @ 256 Mb SDRAM node
4 Kb @ 256 Mb RDRAM node
DRAM Circuit Basics

Sense Amplifier I: 6 rows shown

Sense and Amplify
DRAM Circuit Basics

Sense Amplifier I: 6 rows shown

Vcc (logic 1) Gnd (logic 0)
DRAM Circuit Basics

Sense Amplifier II: Precharged

- Precharged to $V_{cc}/2$
- Sense and Amplify

$V_{cc}$ (logic 1)  Gnd (logic 0)  $V_{cc}/2$
DRAM Circuit Basics

Sense Amplifier III: Destructive Read

1. \( V_{cc} \) (logic 1)
2. Gnd (logic 0)
3. \( V_{cc}/2 \)
4. Sense and Amplify
5. Wordline Driven

- \( V_{cc} \) (logic 1)
- Gnd (logic 0)
- \( V_{cc}/2 \)
DRAM Circuit Basics

“Column” Defined

Column: Smallest addressable quantity of DRAM on chip

SDRAM*: column size == chip data bus width (4, 8, 16, 32)
RDRAM: column size != chip data bus width (128 bit fixed)

SDRAM*: get n columns per access. n = (1, 2, 4, 8)
RDRAM: get 1 column per access.

4 bit wide columns

#0  #1  #2  #3  #4  #5

One Row of DRAM

* SDRAM means SDRAM and variants. i.e. DDR SDRAM
DRAM Architecture Basics

PHYSICAL ORGANIZATION

This is per bank ...
Typical DRAMs have 2+ banks
DRAM “Speed” Part I

How fast can I move data from DRAM cell to sense amp?

$t_{RCD}$

$RCD$ (Row Command Delay)
DRAM “Speed” Part II

How fast can I get data out of sense amps back into memory controller?

$t_{\text{CAS}}$ aka $t_{\text{CASL}}$ aka $t_{\text{CL}}$

CAS: Column Address Strobe
CASL: Column Address Strobe Latency
CL: Column Address Strobe Latency
DRAM “Speed” Part III

How fast can I move data from DRAM cell into memory controller?

\[ t_{RAC} = t_{RCD} + t_{CAS} \]

RAC (Random Access Delay)
DRAM “Speed” Part IV

How fast can I precharge DRAM array so I can engage another RAS?

$\mathbf{t_{RP}}$

$\mathbf{RP}$ (Row Precharge Delay)
DRAM “Speed” Part V

How fast can I read data from two different rows?

\[ t_{RC} = t_{RAS} + t_{RP} \]

RC (Row Cycle Time)
DRAM “Speed” Summary I

What do I care about?

- $t_{RCD}$
- $t_{CAS}$
- $t_{RP}$
- $t_{RC} = t_{RAS} + t_{RP}$
- $t_{RAC} = t_{RCD} + t_{CAS}$

**Definitions:**
- **RAS**: Row Address Strobe
- **CAS**: Column Address Strobe
- **RCD**: Row Command Delay
- **RAC**: Random Access Delay
- **RP**: Row Precharge Delay
- **RC**: Row Cycle Time

- Seen in ads.
- Easy to explain
- Easy to sell
- Embedded systems designers
- DRAM manufacturers
- Computer Architect:
  - Latency bound code
  - i.e. linked list traversal
## DRAM “Speed” Summary II

<table>
<thead>
<tr>
<th>DRAM Type</th>
<th>Frequency</th>
<th>Data Bus Width (per chip)</th>
<th>Peak Data Bandwidth (per Chip)</th>
<th>Random Access Time ($t_{\text{RA}}$)</th>
<th>Row Cycle Time ($t_{\text{RC}}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC133 SDRAM</td>
<td>133</td>
<td>16</td>
<td>200 MB/s</td>
<td>45 ns</td>
<td>60 ns</td>
</tr>
<tr>
<td>DDR 266</td>
<td>133 * 2</td>
<td>16</td>
<td>532 MB/s</td>
<td>45 ns</td>
<td>60 ns</td>
</tr>
<tr>
<td>PC800 RDRAM</td>
<td>400 * 2</td>
<td>16</td>
<td>1.6 GB/s</td>
<td>60 ns</td>
<td>70 ns</td>
</tr>
<tr>
<td>FCRAM</td>
<td>200 * 2</td>
<td>16</td>
<td>0.8 GB/s</td>
<td>25 ns</td>
<td>25 ns</td>
</tr>
<tr>
<td>RLDRAM</td>
<td>300 * 2</td>
<td>32</td>
<td>2.4 GB/s</td>
<td>25 ns</td>
<td>25 ns</td>
</tr>
</tbody>
</table>

Data: Dec. 2002

DRAM is “slow”
But doesn’t have to be $t_{\text{RC}} < 10\text{ns}$ achievable

Higher die cost $\rightarrow$ Not adopted in standard

Not commodity $\rightarrow$ Expensive
Signal Propagation

Ideal Transmission Line

\[ \sim 0.66c = 20 \text{ cm/ns} \]

PC Board + Module Connectors + Varying Electrical Loads

= Rather non-Ideal Transmission Line
DRAM Interface: Protocol

The Digital Fantasy

Pretend that the world looks like this

But...
DRAM Interface: Signals

FCRAM side

Controller side

VDDQ(Pad)

VSSQ(Pad)

DQS (Pin)

DQ0-15 (Pin)

skew=158psec

skew=102psec

*Toshiba Presentation, Denali MemCon 2002
Interface: Clocking Issues

Figure 1: Sliding Time

Figure 2: H Tree?

What Kind of Clocking System?
Path Length Differential

High Frequency AND Wide Parallel Busses are Difficult to Implement
Timing Variations

How many DIMMs in System?
How many devices on each DIMM?
Who built the memory module?

Infinite variations on timing!
DRAM System Topology Determines Electrical Loading Conditions and Signal Propagation Lengths
SDRAM Topology Example

Loading Imbalance
SDRAM Topology Example II

(Same topology, different drawing, a little more detail)
RDRAM Topology Example

Packets traveling down Parallel Paths. Skew is minimal by design.

clock turns around
I/O - Differential Pair

Single Ended Transmission Line

Differential Pair Transmission Line

Increase Rate of bits/s/pin?
Cost Per Pin?
Pin Count?
Increase Rate of bits/s/pin
Packaging

- **DIP**
  - "good old days"

- **SOJ**
  - Small Outline J-lead

- **TSOP**
  - Thin Small Outline Package

- **LQFP**
  - Low Profile Quad Flat Package

- **FBGA**
  - Fine Ball Grid Array

### Target Specification

<table>
<thead>
<tr>
<th>Features</th>
<th>Target</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>FBGA</td>
</tr>
<tr>
<td>Speed</td>
<td>800MBps</td>
</tr>
<tr>
<td>Vdd/Vddq</td>
<td>2.5V/2.5V</td>
</tr>
<tr>
<td>Interface</td>
<td>SSTL_2</td>
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<tr>
<td>Row Cycle</td>
<td>35ns</td>
</tr>
</tbody>
</table>

Memory Roadmap for Hynix NetDDR II
Access Protocol

**Single Cycle Command**

- **Cmd**: $r_0$
- **Data**: $d_0\ d_0\ d_0\ d_0$

**Multiple Cycle Command**

- **Cmd**: $r_0\ r_0\ r_0\ r_0$
- **Data**: $d_0\ d_0\ d_0\ d_0$
Access Protocol (r/r)

Consecutive Cache Line Read Requests to Same DRAM Row

- \(a\) = Active (open page)
- \(r\) = Read (Column Read)
- \(d\) = Data (Data chunk)
Access Protocol (r/w)

One Datapath - Two Commands

Case 1: Read Following a Write Command to Different DRAM Devices

Case 2: Read Following a Write Command to Same DRAM Device

Soln: Delay Data of Write Command to match Read Latency
Address Mapping

Access Distribution for Temp Control
Avoid Bank Conflicts
Access Reordering for performance
Example: Bank Conflicts

Multiple Banks to Reduce Access Conflicts

Read 05AE5700  Device id 3, Row id 266, Bank id 0
Read 023BB880  Device id 3, Row id 1BA, Bank id 0
Read 05AE5780  Device id 3, Row id 266, Bank id 0
Read 00CBA2C0  Device id 3, Row id 052, Bank id 1

More Banks per Chip == Performance == Logic Overhead
Example: Access Reordering

1. Read 05AE5700 → Device id 3, Row id 266, Bank id 0
2. Read 023BB880 → Device id 3, Row id 1BA, Bank id 0
3. Read 05AE5780 → Device id 3, Row id 266, Bank id 0
4. Read 00CBA2C0 → Device id 1, Row id 052, Bank id 1

Act = Activate Page (Data moved from DRAM cells to row buffer)
Read = Read Data (Data moved from row buffer to memory controller)
Prec = Precharge (close page/evict data in row buffer/sense amp)
## Technology Roadmap (ITRS)

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Semi Generation (nm)</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
</tr>
<tr>
<td>CPU MHz</td>
<td>3990</td>
<td>6740</td>
<td>12000</td>
<td>19000</td>
<td>29000</td>
</tr>
<tr>
<td>MLogicTransistors/cm²</td>
<td>77.2</td>
<td>154.3</td>
<td>309</td>
<td>617</td>
<td>1235</td>
</tr>
<tr>
<td>High Perf chip pin count</td>
<td>2263</td>
<td>3012</td>
<td>4009</td>
<td>5335</td>
<td>7100</td>
</tr>
<tr>
<td>High Performance chip cost (cents/pin)</td>
<td>1.88</td>
<td>1.61</td>
<td>1.68</td>
<td>1.44</td>
<td>1.22</td>
</tr>
<tr>
<td>Memory pin cost (cents/pin)</td>
<td>0.34 - 1.39</td>
<td>0.27 - 0.84</td>
<td>0.22 - 0.34</td>
<td>0.19 - 0.39</td>
<td>0.19 - 0.33</td>
</tr>
<tr>
<td>Memory pin count</td>
<td>48-160</td>
<td>48-160</td>
<td>62-208</td>
<td>81-270</td>
<td>105-351</td>
</tr>
</tbody>
</table>

**Trend:** Free Transistors & Costly Interconnects
**Choices for Future**

- **Direct Connect**
  - Custom DRAM: Highest Bandwidth + Low Latency

- **Indirect Connection**
  - Highest Bandwidth
  - Highest Latency

- **Indirect Connection**
  - Inexpensive DRAM

- **Commodity DRAM**
  - Low Bandwidth + Low/Moderate Latency

- **Custom DRAM**
  - Highest Bandwidth + Low Latency
DRAM Evolutionary Tree

(Mostly) Structural Modifications
Targeting Throughput

Interface Modifications
Targeting Throughput

Conventional DRAM

FPM  EDO  P/BEDO  SDRAM  ESDRAM

Structural Modifications
Targeting Latency

MOSYS
FCRAM
VCDRAM

Rambus, DDR/2  Future Trends
DRAM Evolution

Read Timing for Conventional DRAM

- Row Access
- Column Access
- Transfer Overlap
- Data Transfer

Diagram showing the timing for reading data in a conventional DRAM, including RAS, CAS, address, data output, row access, column access, and data transfer.
DRAM Evolution

Read Timing for Fast Page Mode

- Row Access
- Column Access
- Transfer Overlap
- Data Transfer

Diagram showing the timing for read operations in fast page mode, with separate addresses for row (RAS) and column (CAS) accesses, and data transfer at the bottom (DQ), with valid data output indicated at specific times.
DRAM Evolution

Read Timing for Extended Data Out

Row Access
Column Access
Transfer Overlap
Data Transfer

RAS
CAS
Address
Row Address
Column Address
Column Address
Column Address
DQ
Valid Dataout
Valid Dataout
Valid Dataout
DRAM Evolution

Read Timing for Burst EDO

- Row Access
- Column Access
- Transfer Overlap
- Data Transfer
DRAM Evolution

Read Timing for Pipeline Burst EDO

- Row Access
- Column Access
- Transfer Overlap
- Data Transfer

RAS

CAS

Address

Row Address

Column Address

DQ

Valid Data

Valid Data

Valid Data

Valid Data
DRAM Evolution

Read Timing for Synchronous DRAM

(RAS + CAS + OE ... == Command Bus)
DRAM Evolution

Inter-Row Read Timing for ESDRAM

Regular CAS-2 SDRAM, R/R to same bank

ESDRAM, R/R to same bank
DRAM Evolution

Write-Around in ESDRAM

Regular CAS-2 SDRAM, R/W/R to same bank, rows 0/1/0

ESDRAM, R/W/R to same bank, rows 0/1/0

(can second READ be this aggressive?)
DRAM Evolution

Internal Structure of Virtual Channel

Segment cache is software-managed, reduces energy
DRAM Evolution

Internal Structure of Fast Cycle RAM

SDRAM

8M Array (8Kr x 1Kb)

Row Decoder

13 bits

Sense Amps

$t_{RCD} = 15\text{ns}$

(two clocks)

FCRAM

8M Array (?)

Row Decoder

15 bits

$\text{Sense Amps}$

$t_{RCD} = 5\text{ns}$

(one clock)

Reduces access time and energy/access
DRAM Evolution

Internal Structure of MoSys 1T-SRAM

addr

Bank Select

Auto Refresh

$ DQs