Problem one of three

11.16 Consider a ring oscillator consisting of five inverters, each having $t_{PLH} = 60$ ns and $t_{PHL} = 40$ ns. Sketch one of the output waveforms, and specify its frequency and the percentage of the cycle during which the output is high.

Problem two of three

11.17 A ring-of-eleven oscillator is found to oscillate at 20 MHz. Find the propagation delay of the inverter.

Problem three of three

11.26 For a particular DRAM design, the cell capacitance $C_s = 50$ fF, $V_{DD} = 5$ V, and $V_i$ (including the body effect) = 1.4 V. Each cell represents a capacitive load on the bit line of 2 fF. The sense amplifier and other circuitry attached to the bit line has a 20-fF capacitance. What is the maximum number of cells that can be attached to a bit line while ensuring a minimum bit-line signal of 0.1 V? How many bits of row addressing can be used? If the sense-amplifier gain is increased by a factor of 5, how many word-line address bits can be accommodated?