1. Assume the gate propagation delay for each gate is 1 time unit, and draw the timing diagram for all of the gate outputs in response to the input signals (A, B, C) shown.
2. Assume the gate propagation delay for each gate is 1 time unit, and draw the timing diagram for all of the gate outputs in response to the input signals (A and B) shown.

![Diagram of logic gates](image_url)

<table>
<thead>
<tr>
<th>Time in units of gate delay</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
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</tr>
</thead>
<tbody>
<tr>
<td>A</td>
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<td>Y</td>
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</tbody>
</table>

Time in units of gate delay

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
3. Assume the gate propagation delay for each gate is 1 time unit, and draw the timing diagram for all of the gate outputs in response to the input signals (A and B) shown. Assume \( A(t) = B(t) = 0, \ t < 0. \)

![Timing Diagram](image)

Read all of Section 6.8 of Givone and read Sections 7.3.3–7.5.2; then work the following problems:

4. Prob. 6.22.
5. Prob. 6.23.
6. Prob. 6.27.
7. Prob. 6.28.
9. Prob. 7.7.