Electronics

Second Edition

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Clamp Circuits

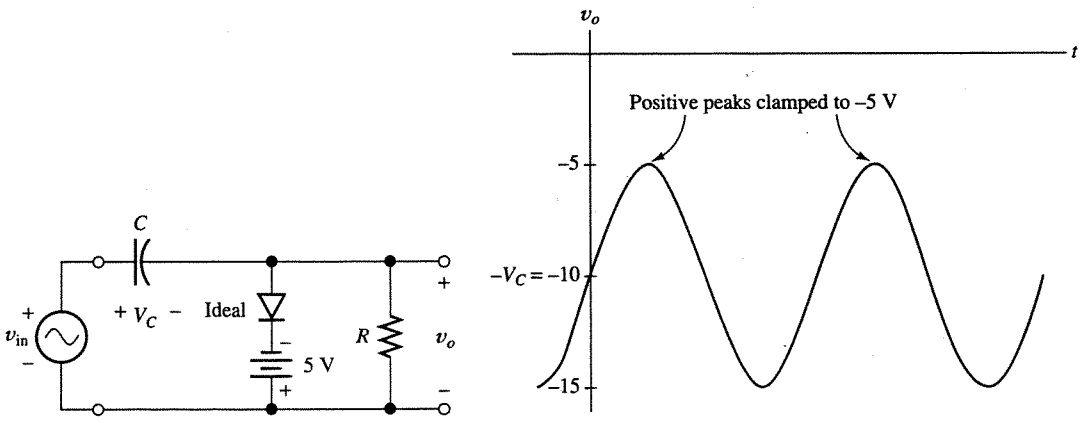
Another diode wave-shaping circuit is the **clamp circuit**, which is used to add a dc component to an ac input waveform so that the positive (or negative) peaks are forced to take a specified value. In other words, the peaks of the waveform are "clamped" to a specified voltage value. An example of a clamp circuit is shown in Figure 3.19. In this circuit, the positive peaks are clamped to −5 V.

The capacitor is a large value, so it discharges only very slowly, and we can consider the voltage across the capacitor to be constant. Because the capacitor is large, it has a very small impedance for the ac input signal. Thus, the output voltage of the circuit is given by

$$v_o(t) = v_{in}(t) - V_C \tag{3.7}$$

If a positive swing of the input signal attempts to force the output voltage to become greater than −5 V, the diode conducts, increasing the value of V_C. Hence, the capacitor is charged to a value that adjusts the maximum value of the output voltage to −5 V. A large resistance R is provided to allow the capacitor to discharge slowly. This is necessary so that the circuit can adjust if the input waveform changes to a smaller peak amplitude.

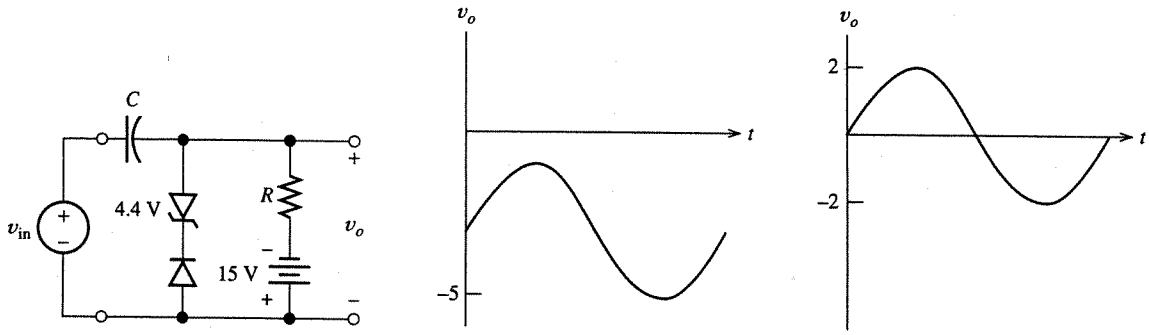
Of course, we can change the voltage to which the circuit clamps by changing the battery voltage. Reversing the direction of the diode causes the negative peak to be clamped instead of the positive peak. If the desired clamp voltage requires the diode to be reverse biased, it is necessary to return the discharge resistor to a suitable dc supply voltage to ensure that the diode conducts and performs the clamping operation. Furthermore, it is often more convenient to use Zener diodes rather than batteries. A circuit including these features is shown in Figure 3.20a.



(a) Circuit diagram

(b) Output waveform for $v_{in} = 5 \sin(\omega t)$

Figure 3.19 Example clamp circuit.



(a) A circuit that clamps the negative peaks to –5 V (an allowance of 0.6 V forward drop is made)

(b) Output for $v_{in} = 2\sin(\omega t)$

(c) Output for $v_{in} = 2\sin(\omega t)$ and R returned directly to ground (diodes do not turn on)

Figure 3.20 See Exercise 3.9.

EXERCISE

3.9 Consider the circuit of Figure 3.20a. Assume that the capacitor is large enough so the voltage across it does not discharge through R appreciably during one cycle of the input.

(a) What is the steady-state output voltage if $v_{in}(t) = 0$?

(b) Sketch the steady-state output to scale against time if $v_{in}(t) = 2\sin(\omega t)$.

(c) Suppose that the resistor is returned to ground instead of -15 V. In this case, sketch the steady-state output against time if $v_{in}(t) = 2\sin(\omega t)$.

Answer (a) For $v_{in}(t) = 0$, we have $v_o = -5$ V. (b) See Figure 3.20b. (c) See Figure 3.20c.

EXERCISE

3.10 Design a circuit that clamps the negative peaks of an ac signal to +6 V. You can use batteries, resistors, and capacitors of any value desired, in addition to Zener or conventional diodes (for both). Allow 0.6 V for the forward drop.

Answer A solution is shown in Figure 3.21.

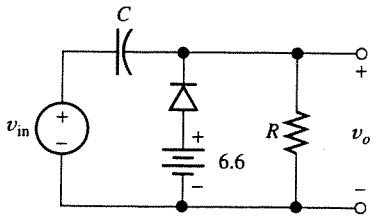


Figure 3.21 Answer for Exercise 3.10.