Design of High-Sensitivity Cantilever and Its Monolithic Integration With CMOS Circuits

Xiaomei Yu, Yaquan Tang, Haitao Zhang, Ting Li, and Wei Wang

Abstract—Rectangular piezoresistive cantilevers with stress concentration holes opened were designed and fabricated in order to increase the response signals of piezoresistive cantilever first. Both the simulations and the measurements on the cantilever sensitivity show that this design can obviously result in an improvement on the displacement sensitivity of the piezoresistive cantilever. After a characterization study on the piezoresistive cantilever, a monolithic integration of the microcantilever array with a complementary metal–oxide–semiconductor (CMOS) readout circuitry based on the silicon-on-insulator (SOI) CMOS and the SOI micromachining technologies was designed. A cantilever array, a digital controlled multiplexer, and an instrumentation amplifier compose the integrated sensor system, and post-CMOS process was designed to fabricate the integrated system. The measurement results on the SOI CMOS circuitry of the integrated system prove a feasibility of the integration design.

Index Terms—Cantilever, monolithic integration, post-CMOS process, silicon-on-insulator (SOI) CMOS.

I. INTRODUCTION

SINGLE-CLAMPED suspended beams (cantilevers) are some of the simplest microelectromechanical systems (MEMS) transducer. The small size of the microcantilever and the precise measure of the induced deflection permit the detection of small surface stress. As recent research efforts have advanced in several converging areas of science and technology, physical, chemical, and biological sensors based on cantilever technology were developed. Cantilever-based sensors have been proved to be quite versatile and sensitive devices and have been used mainly in biochemical sensors recently [1]–[11]. Changes in the surface properties of the microcantilever through binding or hybridization of analytes to receptor molecules will directly influence its surface stress. This causes the microcantilever to deflect and the deflection is proportional to the analytes concentration.

The microfabricated cantilevers can be operated as detectors of surface stresses and resonance frequency. In surface stresses mode, the cantilever will bend with a nanometer accuracy; therefore, the readout system is an important part for cantilever sensors. Several examples of surface stress sensors have been demonstrated with 10^{-5} N/m stress sensitivity and have been

Fig. 1. Layout of a Wheatstone Bridge that is composed of four piezoresistors.

demonstrated for detection of alcohols, proteins, and amino-nucleotides [13]–[16]. Using optical, piezoresistive, piezoelectric, capacitance, or electron tunneling methods, cantilever deformations can be measured with sufficient precision. Piezoresistive transducers are widely adopted in measuring cantilever bending due to the simple electrical output measurement and easier to be integrated with integrated circuits (ICs).

In piezoresistive readout cantilever, the relation between the relative resistance change and the surface stress suggest clearly that increasing the stress level will increase the relative resistance change, and therefore the cantilever-based sensor sensitivity. The displacement sensitivity of piezoresistive cantilever is described by the following expression [8]:

$$\frac{\Delta R}{R} = \frac{(\sigma_1 - \sigma_2)}{D} \quad (1)$$

where $\Pi = \beta(3\pi_L(1 - \nu)/t)$ is the piezoresistor coefficient, D is the vertical displacement of the cantilever, π_L is the longitudinal piezoresistive coefficient of silicon, σ_1 and σ_2 are the longitudinal stress and transverse stress, respectively, t is the cantilever thickness, ν is the Poisson ratio, and β is a factor that adjusts for the thickness of the piezoresistor. The displacement sensitivity of piezoresistive cantilever is proportional to the differential stress ($\sigma_1 - \sigma_2$), therefore, the deflection signal can be increased by maximizing the differential stress.

The need for an integration of the MEMS devices with the integrated circuitry is crucial for communicating and transducing the minute signals to the macroscopic world. There is documented evidence of microcantilevers integrated with a signal conditioning circuitry for detecting different kinds of physical or chemical properties [17], [18]. Generally speaking, MEMS–IC integration can be categorized in to two groups; hybrid integration and monolithic integration. In the case of hybrid integration, MEMS parts and circuit parts are fabricated separately and then packaged together by wafer bonding or other packaging

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NODAL SOLUTION
STEP=1
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SEQV      (AVG)
DMX =3684
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Fig. 2. ANSYS top view of stress contour for the designed cantilever.

technologies. With regard to the micro-to-nanometer-scale signals of cantilever sensors, monolithic integration is preferred. The main contributions of monolithic integration are the decrease of the system bulk and cost, the increase of the device reliability, and elimination of parasitic capacitance introduced by the external bonding pads and wires. The complementary metal–oxide–semiconductor (CMOS) circuitry for the readout of the cantilever deflection integrated together with the cantilever by using a monolithic technology will permit *in situ* and smart detections of the minute information.

This paper provides a method of increasing cantilever surface stress through introducing stress concentration holes first. Then a monolithic integration of the microcantilevers and the CMOS circuitry by using both the silicon-on-insulator (SOI) CMOS and the SOI micromachining technologies is provided. This integration method leads to not only the feasibility of fabrication, but also to circuit improvements in power consumption, the signal-to-noise ratio, signal loss, and so on [19], [20].

II. DESIGN AND SIMULATION

A. Cantilever

In piezoresistive cantilever, the change in the resistivity can be conveniently measured by using a Wheatstone Bridge. Four piezoresistors make up the Wheatstone Bridge (Fig. 1), two of them are located on the substrate, the third is on the reference cantilever, and the fourth on the measurement cantilever. A differential voltage signal from the Wheatstone Bridge will record the information that occurred on the measurement cantilever. Based on our former experiment results [6], [12], the cantilever beams in this work are designed to be $200\ \mu\text{m} \times 50\ \mu\text{m}$ and $150\ \mu\text{m} \times 40\ \mu\text{m}$ in length and width with a thickness of $0.6\ \mu\text{m}$. Looped piezoresistors in one leg's dimension of $100\ \mu\text{m} \times 15\ \mu\text{m}$ are placed on the measurement and reference cantilevers, respectively. The piezoresistor layer is realized by a boron-ion implantation with an estimated depth of $0.2\ \mu\text{m}$.

In order to concentrate the surface stress, six rectangular holes with the dimension of $10\ \mu\text{m} \times 5\ \mu\text{m}$ are opened on the piezoresistors' legs. The geometrical discontinuity caused by the holes will change the stress contours and maximize the stress in the hole regions. The maximized stress difference will result in an increasing on the cantilever sensitivity.

ANSYS finite element software has been used as a tool to model the mechanical properties of the designed cantilever first. The analysis performed here use only the surface stress of the cantilever and the depth effects at the piezoresistive sensing regions are ignored for simplification. For the ANSYS simulation described in this paper, Young's modulus of $1.6 \times 10^{11}\ \text{Nm}^{-2}$, Poisson's ratio of 0.22 and density of $2.28 \times 10^3\ \text{kg m}^{-3}$ for silicon are used. The finite element mesh is simplified with the element type of shell and static analysis. All the loads are applied at the end of cantilever with a pre-pressure of 0.5 MPa. The assumptions of temperature and material uniformity are made in the FE model.

Fig. 2 shows the top view of a two-dimensional (2-D) plot of ANSYS von-Mises stress contour for the designed cantilevers [12]. The stresses showed on the ruler increase from left to right. It can be seen clearly from the simulated figure that the stresses decrease gradually from the anchor edge (left) to the end line (right), and are maximized around every holes region as expected.

The differential stress distributions of longitudinal and transverse and the vertical displacement along the longitudinal axes for the cantilevers are shown in Fig. 3 [13]. In order to make the comparisons, an ordinary rectangular cantilever with the same dimension and modeling parameters are also modeled in Fig. 3. "Peaks" are observed at every holes opened position, and the stresses near the holes region increase or decrease sharply. Obviously, the stresses can be localized near every region by adding holes. Between every two adjacent peaks, minimum stress regions are observed, which are almost in the same stress level as those of the ordinary rectangular cantilevers. The simulated

Fig. 3. Stress distribution and vertical displacements of cantilevers along the longitudinal axis.

stresses near the hole regions are about 1.5 times higher than that of the rectangular cantilever at the same distance position. The displacement sensitivities are calculated with (1) by reading out the vertical displacement and the differential stresses of the cantilevers from Fig. 3. The maximum displacement sensitivity is calculated to be 2×10^{-5} MPa/nm for the cantilever with a dimension of $200 \mu\text{m} \times 50 \mu\text{m}$. Compared with the ordinary rectangular cantilevers, the simulated increases of displacement sensitivities for the cantilevers with holes opened is 30%.

B. Integration

The monolithically integrated sensor system consists of two Wheatstone Bridges, a multiplexer, and an instrumentation amplifier. Fig. 4 shows the schematic diagram of the readout circuitry along with the two Wheatstone Bridges. The differential voltage signals from the Wheatstone Bridges are first input into a time-division multiplexer. The multiplexer controlled by a digital clock works as a function of collecting multisignals from different sensors and transfers them into the amplifier. Therefore, those signals from different sensor channels can be detected with the instrument amplifier at different time. A two-stage cascode symmetrical operational transconductance amplifier (OTA) was selected to implement the voltage amplification because of its relatively high amplification coefficient, high output wing, low noise, and simple architecture. The first stage of the two-stage instrumentation amplifier is made up of the sub-amplifier A1, subamplifier A2, and their proportional resistors R1, R2, and R3, while subamplifier A3 and its proportional and feedback resistors R4, R5, R6, and R7 build the second stage of the amplifier.

Fig. 4. Schematic diagram of the integrated sensor system.

Fig. 5. Layout of body contact design.

Fig. 6. SEM photograph of a finished cantilever array.

SOI wafer is a preferred wafer to fabricate the high-sensitivity single-crystal silicon (SCS) cantilevers and the CMOS circuits. In considering the previous references, integrations of microcantilevers with readout circuits were mostly made on SOI wafer by the bulk-silicon CMOS technology. In bulk-silicon CMOS designs, the device layer and the buried oxide layer are removed in order to build the CMOS circuits on the handle silicon. The p- or n-type MOS transistors are isolated from each other by the well layer. The latch-up effect and the big parasitic

Fig. 7. Fabrication processes for the monolithically integrated system with post-MEMS processes.

capacitances of the bulk-silicon CMOS devices would result in a low transfer velocity and a high signal-to-noise ratio for the readout circuits. Furthermore, the bulk-silicon CMOS processes are complicated.

In contrast, SOI CMOS makes use of the buried oxide layer to isolate the devices from the substrate and the field oxidation to isolate the devices from each other, which make great improvements in the parasitic capacitances, the latch-up effect, and the short channel effect compared with bulk-silicon CMOS circuitry. The elements that have a thin SOI layer (normally < 50 nm) and have all body areas under the channel depleted, are called fully depletion (FD) type SOI. Conversely, elements that have a thick SOI layer (normally > 100 nm) and have some areas at the bottom of the body area that are not depleted, are called partial depletion (PD) type SOI. A PD SOI device has advantages in fabrication simplicity, higher threshold voltage, small channel current leakage, etc., therefore, PD SOI CMOS technology together with the SOI micromachining processes were adopted in our integration design. A disadvantage in PD SOI CMOS is the kink effect. Kink effect is an undesirable increase of I_{DS} at high drain-source voltages on SOI PD NMOS transistor, which can be explained by the impact ionization occurring in the high-field region at the drain end of the channel. This effect can be avoided by using a body contacts design, which leads the hole charges in the body region into the source end. Fig. 5 shows the layout of the body contact design in our SOI CMOS circuitry.

III. FABRICATION

The cantilevers with the concentration holes opened were fabricated from a SOI wafer using a series of front-side definition and backside wet and dry etching. The detailed fabrication processes can be found in [12], and a scanning electron microscope (SEM) photograph of the cantilever array is given in Fig. 6 [12].

Based on the standard SOI CMOS and the MEMS processes, post-MEMS processes were designed as a manufacturing solution for the monolithic integration, and the fabrication processes are depicted in Fig. 7. Single-crystalline silicon of p-type has the biggest piezoresistive coefficient in $\langle 100 \rangle$ orientation, therefore a SOI wafer with 0.2- μm silicon device layer (p-type, in $\langle 100 \rangle$ orientation) and 400-nm box oxide layer was used for the fabrication. Apart from the cantilever releasing, a standard SOI CMOS technology was used in most processes including defining the active and field regions (a); the light dopings of boron and phosphorus ions in order to adjust the threshold voltage (b); depositing polysilicon and patterning the polysilicon gate (c); the heavy dopings of boron and phosphorus ions forming the source and drain regions, and the piezoresistors on Wheatstone Bridges were defined at this step (d); insulating the circuits with SiO₂, and electrically activating the doping (e); sputtering Al, and patterning the metal wires (f). After the CMOS processes with the metal wires both for circuits and Wheatstone Bridges were patterned, the cantilever patterns were defined. Finally, deep reactive ion etching under

Fig. 8. A die photograph of the integrated sensor.

Inductively coupled plasma (ICP) system was applied to release the cantilevers from the front side (g), and the buried oxide together with the insulating layer of CMOS circuits served as an encapsulation layer of the cantilevers. Fig. 8 gives a die photograph of the integrated sensor. The stress mismatch of the cantilever layers makes the cantilever bending, and therefore the cantilevers look a little dark under optical microscope.

IV. MEASUREMENT RESULTS

Experimental studies of the cantilever deflection sensitivity were accomplished by pushing the cantilever with a microprobe, and reading out the cantilever deflections by a micrometer. The microprobe exerts a force on the cantilever end, resulting in a cantilever vertical displacement, and then a resistance change of the piezoresistor.

Two measurement relations between the relative resistance changes ($\Delta R/R$) and the vertical deflections (D) at the cantilevers end are shown in Fig. 9 [12]. In order to make the comparisons, ordinary rectangular cantilevers without holes opened and with the same dimensions were also measured and plotted on Fig. 9, respectively. Obviously, the relative resistance changes of the cantilevers with holes opened are higher than that of the ordinary rectangular cantilevers. By using the fitted line slope, the deflection sensitivity ($(\Delta R/R)D^{-1}$) of $3.4 \times 10^{-6} \text{ nm}^{-1}$ for the cantilevers with the holes opened and $2.6 \times 10^{-6} \text{ nm}^{-1}$ for the ordinary rectangular cantilevers are obtained. The deflection sensitivity for the cantilevers with the concentration holes designed is 1.3 times of the ordinary rectangular cantilevers, and this result is almost the same as the simulations. The minimum detectable deflection (MDD) for the cantilever with holes opened is calculated to be 0.1 nm at a 6-V biased voltages and a 1-kHz measurement bandwidth [6].

Fig. 9. Relative resistance changes versus cantilever deflections for the cantilevers with the dimension of $200 \mu\text{m} \times 50 \mu\text{m}$ (a) and $150 \mu\text{m} \times 40 \mu\text{m}$ (b).

Fig. 10. Test result of transfer curves for NMOS (a) and PMOS (b) transistors.

The characteristics of the SOI CMOS circuit for the integrated system were studied basically. Fig. 10 presents the test results of the transfer curves of a SOI-NMOS and a SOI-PMOS device with a width-to-length ratio of 50/20 and at a 0-V substrate biased voltage. It can be seen from this figure that both the SOI-NMOS and the SOI-PMOS devices work well in the saturated regions. As the V_{GS} increases, the slopes of $I_{DS} \sim V_{GS}$ curves in linear regions change a little, and this is due to the hot carrier mobility degradation under a biased voltage. The threshold voltages were measured to be $+0.84 \text{ V}$ and -0.84 V

Fig. 11. Input and output curves for NMOS devices without (a) and with (b) body contact designed.

Fig. 12. Test result of input and output curve of a subamplifier.

for the SOI-NMOS and the SOI-PMOS devices, respectively, and which are almost the same as the simulation results.

Fig. 11 shows the comparison results of the input and output characteristics for SOI-NMOS devices without and with the body contact designed at different gate-source voltages. Obviously, the kink effect on the SOI-NMOS device is totally avoided with the body contact designed, and the NMOS transistor with body contact designed works very well in the saturated region. The input and output curves of a subamplifier through a dc voltage sweep is shown in Fig. 12. The input voltage range is ± 0.3 V, and the output voltage amplitude is from -1.22 to 1.1 V. The subamplifier has a triple times voltage amplification for a dc signal, which is also the same as in our design.

V. CONCLUSIONS

This work has described designs of a silicon-based piezoresistive cantilever and its monolithic integration with CMOS circuits based on the SOI CMOS and the SOI micromachining technologies. Holes are designed on the piezoresistive regions of the cantilevers, and the measurement results on the cantilever

displacement sensitivity show a 1.3 times increase. Therefore, these cantilevers with stress concentration holes opened can result in a stress concentration. A full on-chip integration using post-CMOS processes was designed and processed. The test results on the SOI CMOS circuits proved the feasibility of the monolithic integration.

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