Synthesis Project 1: A Few ALUs

ENEE 646: Digital Computer Design, Fall 2008
Assigned: Tuesday, Sep 30

Purpose

This project is intended to help you understand the difference between various module constructs. Any particular function can be implemented in a large number of ways, and each different implementation can produce a dramatically different result when you synthesize it.

Synthesis

Start up the synthesis package by typing the following on a departmental server:

```
> tap synopsys
> design_analyzer &
```

This will set up the necessary path to get at the synopsys applications, and it will invoke a GUI-based front-end to their various synthesis packages.

Download the file "s1examples.v" from the course website, put it into your working directory, and run the following commands within design_analyzer:

```
File -> Analyze (choose the s1examples.v file)
File -> Elaborate (each of the aluX designs in turn)
```

You can speed things up by creating another module (e.g. "top") that simply instantiates the various aluX modules, which will allow you to perform only one Elaborate command. Look at each design in turn, comparing the final results to the source code.

Assignment

Write up your conclusions: what Verilog constructs become what circuits when synthesized?

Begin looking at how you can improve your project 1 in terms of synthesis: that will be your next synthesis project.