Problem 1

H&P 1.4

Problem 2

H&P 1.16

Problem 3

In lecture, we reviewed a 5-stage MIPs pipeline that provides bypassing to the execute stage (handout #4, page 10). However, interlocks are needed since the bypass wires cannot forward between a load instruction and an immediately following instruction that depends on the load (requiring a 1-cycle stall). The stall condition for this interlock is:

\[
Stall_{all-loads} = ((RS1 = RD_E) \times re1) + ((RS2 = RD_E) \times re2) \times (IR_E, op = LW)
\]

(Assume \(re1\) and \(re2\) are asserted when an instruction reads the first or second source register specifier, and that these signals are the same as the ones given in lecture).

It is possible to bypass a load followed by a dependent store since the store doesn’t need the result of the load until the beginning of its memory stage. For instance:

\[
\begin{align*}
\text{LW R1, 0(R2)} & \quad [RS1 = R2, RD = R1] \\
\text{SW R1, 0(R3)} & \quad [RS1 = R3, RS2 = R1]
\end{align*}
\]

Modify the pipeline in Figure 1 below to eliminate the interlock in the above instruction sequence by adding a 2-to-1 MUX and making some wiring changes.
Give the logic equations for controlling the new 2-to-1 MUX, and the new stall signal:

\[ MUX_{select} = \]

\[ Stall_{new} = \]

**Problem 4**

H&'P C.5, parts a. through e.