Memory Subsystem Architecture

64M x 4 x 8bits

2Gb per chip
4 x 256MB = 1Gbytes per rank
Memory Transaction

Single Memory Access:

\[ t_{\text{address}} = 10\text{ns} \]
\[ t_{\text{data access}} = 50\text{ns} \]
\[ t_{\text{data transfer}} = 10\text{ns} \]

Total access latency = \( 70\text{ns} \)

Interleaved Memory Access:

Address Bus: ADDR1 ADDR2

Bank 0:

Data Access

Bank 1:

Data Access

Data Bus: Data 1 Data 2

\[ \text{Memory bandwidth} = \frac{W}{\text{total latency}} = \frac{W}{(t_{\text{address}} + t_{\text{data access}} + t_{\text{data transfer}})} \]

assuming no bank conflicts

bandwidth = \( \frac{W}{t_{\text{data transfer}}} \)
Low-Order Interleaving

How many banks are needed?

Address Bus

Bank 0

Bank 1

Bank 2

Bank 3

Bank 4

Bank 5

Data Bus

number of banks = \( \min(\frac{T_{\text{data\_access}}}{T_{\text{data\_transfer}}}, \frac{\text{block\_size}}{W}) \)
DRAM Architecture

EDO DRAM:

DRAM page size typically the square root of DRAM size

\[ \text{e.g. } 64 \text{ Mbit DRAM} \Rightarrow 8 \text{ Kbits} \]

\[= 1 \text{ Kbyte} \]

Lots of data in a DRAM page

ADDR:

\[
\begin{array}{llll}
\text{ROW} & \text{COL1} & \text{COL2} & \text{COL3} \\
\end{array}
\]

DATA:

\[
\begin{array}{llll}
\text{Data 1} & \text{Data 2} & \text{Data 3} \\
\end{array}
\]
DRAM Architecture

CDRAM:

Multiple internal banks:

I/O Pins