

Course Syllabus
ENEE 464: Digital Computer Design, Spring 2005
Prof. Peter Petrov

1. Basic Information

Time and Place

Lecture: TuTh 2:00pm – 3:15pm, EGR 0135

Professor

Peter Petrov: AVW-1421, ppetrov@ece.umd.edu

Office hours: TuTh 11:00a-12:00a

Class Home Page: <http://www.enee.umd.edu/class/enee446-1>

2. Course Overview

This course covers the architecture and design of microprocessors, memory hierarchies, and touches upon system-level software. It is intended to give you a solid understanding of how digital computers are implemented today. We will cover concepts such as pipelines, caching, branch predictors, virtual memory, superscalar execution, very-long-instruction-word architectures (VLIW), precise interrupts, and low-level operating system mechanisms. You will learn these concepts by not only reading about them but by implementing some of them; you will partially design and implement a simple microprocessor at various levels of sophistication. You will first implement a simple processor, then a pipelined machine, and then you will have the opportunity to improve on a design reflecting current thinking in high-performance microprocessors. Implementing in this course will mean coding your design using the Verilog hardware description language (HDL). Describing and simulating your design in Verilog forces you to be much more precise in terms of hardware implementation details and structure. Consequently, this gives you a better understanding of how your design works and the ramifications of your design choices.

3. Prerequisites

Students must have taken ENEE 244 and ENEE 350, or have equivalent knowledge of digital logic design and computer organization. You should understand digital design concepts such as multiplexers, gates, boolean algebra, finite-state machines, and flip-flops. You should understand fundamental computer organization: what the program counter is, what a register file is for, how buses are used, what happens in the hardware to effect instruction execution, etc. It would help if you also understand and are reasonably fluent in programming C, because Verilog is very C-like.

4. Course Material

The required text for the course:

Computer Architecture: A Quantitative Approach, 3th Ed., by Hennessy and Patterson.

This is a widely used textbook that describes in reasonable detail most of today's thinking in high performance architecture. It is a good book and is valuable as a desktop reference.

Verilog language manuals will be provided in an electronic form.

5. Class Projects

Three projects will be assigned during the course. Each of these project assignments will require a substantial effort on your part.

Project 1: Verilog implementation of a simple CPU

Project 2: Verilog implementation of a pipelined CPU

Project 3: Precise interrupts support, hardware and software support for virtual memory

As each project assignment requires a significant amount of work for design and verification, please plan accordingly and start working on each project as soon as it is announced and its description and requirements are made available to you. Projects are due at 8pm on the due date. A default extension of two days will be given with a penalty of 20% of your project grade.

Extension requests (other than the default two days extension) will be considered only if you ask the professor before the original due date. Extensions will only be granted for medical or personal emergencies. Be prepared to substantiate any extension request you make with written proof, for example a written note from your doctor.

All work on projects is to be your own. Violation will result in a zero on the project or exam in question and initiation of the formal procedures of the Student Honor Council. You are not allowed to discuss or made available to other students any implementation details and source code from the projects.

6. Homeworks

Homework problems will be assigned occasionally. The purpose of the homework problems will be to prepare you for the midterm exams and the final exam. Homework assignments will be neither collected nor graded.

7. Exams

You are required to take the midterm and the final exams at the scheduled times. Unless a documented medical or personal emergency is involved you will get zero credit for missing the exam. If you expect to have conflicts with the scheduled exam time you should contact the instructor at least 4 weeks in advance. All exams will be closed notes, closed books.

8. Grading Policy

The final class score will be computed as a weighted sum of your scores on the projects and the exams. Each of these will have the following weights.

Project 1, due <i>Feb 22</i> :	5%
Project 2, due <i>March 17</i> :	10%
Project 3, due <i>April 28</i> :	15%
Midterm1, <i>March 3</i> :	20%
Midterm2, <i>April 12</i> :	20%
Final exam, <i>May 19</i> :	30%

9. Special needs

If you have a documented disability, please contact me as soon as possible.