ENEE417 Final Lab Report:  
Power Amplifier Design

Introduction

The objective of this lab experiment was to design, fabricate, analyze, and test an original audio power amplifier. A power amplifier circuit is used to increase the performance of the sound source, thus making it louder. In general, the purpose of an amplifier is to take an input signal and make it stronger or increase its amplitude. So a fairly high-quality audio amplifier takes in a small signal and amplifies it to sufficiently drive a speaker, without distorting the original signal. The power amp makes sure that there is enough current so the load does not “sag” the voltage at the output. Power amplifiers are used for high performance power management. They can very easily take an ordinary sound system and make it an extraordinary sound system.

The project was very informative. It is very important to experience the design and thought process of an engineer. It is also good to see how things work theoretically and physically because it makes troubleshooting easier. Power amplifiers and projects of this nature are all about making things better, stronger, and more durable. Therefore, designs are always being implemented, innovated, and changed to preserve the future.

There are probably better alternatives than building power amplifiers, such as paying for a great amplifier that costs five times as much. However, a lot can be learned from building a power amp circuit from scratch. It lays out the fundamentals of design and there is really no substitute to hands on experience. There are many factors that can come into play when problems occur. Only by designing and building from experience, can one realize potential faults in designs.

P-SPICE Cadence was used to design the power amp circuit. From the simulation, different measurements were taken to analyze the output of the circuit. After certain design specifications were met, the circuit was physically built on a bread board to test with active parts. After testing on the bread board was completed, the circuit was then built on a PCB board. This report will discuss the performance of the constructed power amp, and compare the actual, physical characteristics to the ones obtained through PSPICE.
Power Amplifier Circuit

The proposed audio power amplifier design consists of two stages: common emitter and emitter follower. The common emitter amplifies the small input signal and the emitter follower provides the necessary current to the load without sagging the voltage. Instead of using a single ended common emitter stage, it was decided to use a differential pair. The point of using a differential pair is that this way the common emitter stage is much less sensitive to noise and interference than a single-ended circuit. Also, to increase input impedance 5457 JFETs were used in the differential pair. Complete amplifier design is presented in Figure 1 below.

Figure 1: Power Amplifier Schematic
Figures 2 and 3 below show DC voltages and currents as predicted by PSPICE.

Figure 2: PSPICE DC Voltages

Figure 3: PSPICE DC Currents
As one can see from Figure 4, in audible frequency range input impedance is approximately 100 kΩ. Ideally it would be desired for input impedance to be infinite, or at least several hundred kilo-ohms. However, to achieve greater input impedance the amplifier design would need to be significantly more complicated, which is not desired for this lab. Figure 5 shows a flat frequency response from 20 Hz to 20 kHz for input impedance phase. This is a desired characteristic of the amplifier.
From figure 6 one can see that in audible frequency range the output impedance is around 1.5 Ω. Ideally it is desired for output impedance to be zero. However, considering that the amplifier design is by no means a state-of-the-art hi-fi amplifier, output impedance of 1.5 Ω is close enough. Figure 7 illustrates the phase frequency response of output impedance. Just as with the case of input impedance, the phase response is flat in audible frequency range.

![Figure 6: Output Impedance Amplitude vs. Frequency (log-log plot)](image)

![Figure 7: Output Impedance Phase vs. Frequency (linear-log plot)](image)
Open loop gain of the amplifier is roughly 75 in the audible frequency range, and remains flat throughout. The phase of the open loop gain remains flat as well. Plots of open loop gain amplitude vs. frequency and open loop gain phase vs. frequency are shown in Figures 8 and 9 below.

**Figure 8: Open Loop Gain Amplitude vs. Frequency (log-log plot)**

**Figure 9: Open Loop Gain Phase vs. Frequency (linear-log plot)**
The closed loop gain of the amplifier is 15. Figure 10 shows the frequency response of the amplifier closed loop gain magnitude. As one can see, not only does the gain remain constant from 20 Hz to 20 kHz, but also below 20 Hz and above 20 kHz. The gain starts losing its flat characteristic below 5 Hz and above 150 kHz. Figure 11 shows that the closed loop gain phase also remains flat in the audible frequency range. However, unlike the gain amplitude, gain phase does not remain flat below 20 Hz and above 20 kHz.
The PCB layout of the power amplifier is presented in Figure 12. The layout was created with Microsoft Paint, and was designed so that there are no jumper wires. This makes the PCB look neat and also makes the circuit easier to trouble shoot, because there is no question of whether jumper wires have good connections.

Figure 12: Power Amp PCB Layout

Aside from building the power amplifier, an equalizer (EQ) circuit was also designed. The PSPICE schematics of the circuit are shown in Figure 13 below.

Figure 13: EQ Schematic
Figure 14: EQ Wiring Diagram

Figure 14 shows the wiring diagram of the EQ circuit. The EQ circuit consists of a high pass and a low pass filter the outputs of which are then summed together by an op-amp summer. Both filters have a potentiometer that allows adjustment of treble and bass in the signal. Figure 15 presents a PCB layout of the EQ circuit.

Figure 15: EQ PCB Layout
Experiment

The actual power amplifier that was built differed from the one simulated in PSPICE. When the amplifier was built on a breadboard the output had a large DC offset and the output was clipping. Because of this, some resistor values were changed to adjust the biasing and the feedback of the power amplifier. Also, the feedback resistor was replaced with a potentiometer so as to allow any adjustments to the circuit. Figure 16 shows the actual resistor values and measured DC voltages of the final circuit. Notice that the DC offset is -23 mV which is acceptable for the low-fi amplifier that was built in this lab.

Figure 16: Constructed Power Amp with DC Voltages
Figure 17: Gain Amplitude & Phase vs. Frequency

The graphs in Figure 17 above were created with LabView. The top graph in Figure 17 shows gain amplitude vs. frequency log-log plot, and the bottom graph in Figure 17 shows gain phase vs. frequency linear-log plot. The amplitude vs. frequency plot has a steady ripple. The reason for this ripple is the 60 Hz noise from the power supply rails of the circuit. To remove these oscillations coupling capacitors would need to be inserted between the circuit and the supply rails. The phase vs. frequency graph seems to have a great slope. However, if one looks at the y-axis, he will see that the reason for this seemingly great slope is the scale distortion of the y-axis.

To find the input impedance of the built circuit, a 100 kΩ resistor was placed at the input of the power amplifier, and the output of the amplifier was grounded. Voltage was measured before the 100 kΩ resistor (call it \(V_i\)) and between the 100 kΩ resistor and the power amplifier circuit (call it \(V_1\)). Since current is supposed to be continuous, the following relation applies:

\[
\frac{V_i - V_1}{R} = \frac{V_1}{R_{ip}},
\]

where \(R\) is the 100 kΩ resistor and \(R_{ip}\) is the input impedance. The measured values were: \(V_i = 177\) mV, \(V_1 = 96.2\) mV, and \(R = 100\) kΩ. Solving for \(R_{ip}\):
R_{ip} = V_1R / (V_i - V_1) = 96.2 \text{ mV} \times 100 \text{ k}\Omega / (177 \text{ mV} - 96.2 \text{ mV}) \approx 119 \text{ k}\Omega. \text{ This value is close to what was obtained with the PSPICE simulations, which yielded input impedance of } 100 \text{ k}\Omega.

The output impedance was a bit trickier to measure. First, the 8 \text{ } \Omega \text{ load resistor on the power amplifier output was replaced with a 100 k}\Omega \text{ resistor. The reason for this is that most of the potential drop would occur over the 100 k}\Omega \text{ resistance and not the power amplifier. The potential before the 100 k}\Omega \text{ resistor (call it } R \text{) was measured, and found to be 6.43 V. Since the resistance of the power amplifier becomes negligible compared to the 100 k}\Omega \text{ resistance, the potential before the amplifier should equal the potential before the 100 k}\Omega \text{ resistance. Next step was to replace the 100 k}\Omega \text{ resistance with 25 } \Omega \text{ resistive load. Voltage before the 25 } \Omega \text{ load was measured and found to be 5.72 V (call this value } V_i). \text{ Based on continuity of current, the following relation holds: } (V_o - V_i)/R_{out} = V_i/R, \text{ where } V_o \text{ is voltage before the amplifier, } V_i \text{ is voltage before the resistive load at the output, } R_{out} \text{ is the output impedance, and } R \text{ is the resistive load of the amplifier. Solving for } R_{out}: R_{out} = R (V_o - V_i)/V_i = 25 \Omega \times (6.43 \text{ V} - 5.72 \text{ V})/5.72 \text{ V} = = 3.10 \text{ } \Omega. \text{ The PSPICE simulations predicted output impedance of 1.5 } \Omega, \text{ and the actual output impedance of the amplifier is 3.10 } \Omega. \text{ Although the output impedance might seem a bit high, one needs to remember that there is a lot of room for experimental error, and that the actual output impedance might be a bit lower than measured with the crude method described above.}

In Figure 18 one can see the photograph of the actual power amp circuit constructed during the lab. Figure 19 presents the photograph of the equalizer PCB board.

![Figure 18: Actual Power Amp PCB](image-url)
Discussion and Conclusion

One great revelation that took place in the course of building and testing the power amplifier circuit was that simulation results yielded by PSPICE can be far from correct when dealing with discrete circuits. PSPICE provides a general idea of the behavior of the circuit. To get the circuit to work correctly on the board one needs to alter resistance values and sometimes some of the circuit topology to get low DC offset for the output voltage, and prevent the signal from clipping.

Some of the improvement that could be made to the constructed circuit would be the inclusion of capacitors between the supply rails and the circuit to isolate the 60 Hz ripple that was observed with LabView. Also, it would nice to add a third tone control to the EQ circuit to regulate the midrange of the signal.

Overall, the lab provided a good experience designing and troubleshooting discrete circuitry. As an improvement to the lab, it would be good to see positives and negative of various amplifier classes discussed in lecture (e.g. differences between classes A, AB, and D amplifiers). Also it would be a good idea to have several reference designs posted on the web for students to choose from.