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Damascene Process and Chemical Mechanical Planarization

The constant demand to scale down transistors and improve device performance has led to material as well as process changes in the formation of IC interconnect. Traditionally, aluminum has been used to form the IC interconnects. The process involved subtractive etching of blanket aluminum as defined by the patterned photo resist. However, the scaling and performance demands have led to transition from Aluminum to Copper interconnects.

The primary motivation behind the introduction of copper for forming interconnects is the advantages that copper offers over Aluminum. The table 1 below gives a comparison between Aluminum and Copper properties.

	Aluminum	**Copper**
Electrical Resistivity	2.65μΩ-cm	1.68μΩ-cm
Thermal Conductivity	238W/m-K	394W/m-K

Table 1: Comparing Aluminum and Copper properties [3]

The table 1 shows that the electrical resistivity of Copper is much smaller than Aluminum. The smaller resistivity translates into smaller line resistances, which in turn translates into smaller RC delay. Smaller RC delay means the speed performance of the devices increases. Secondly as, resistivity decreases, Joule Heating also decreases.

Joule Heating, $Q = J^2 \rho$

So as resistivity ρ decreases, Q decreases. This means that for the same amount of Joule Heating, we can have larger current densities, J. Larger values of current density means that we can have smaller areas, i.e. we can scale down the devices even more. Thirdly copper has larger activation energy than aluminum. Electromigration, a critical reliability issue, is largely dependent on the activation energy of the metal. Electromigration mean-time-to-failure (MTF) is directly proportional to the exponent of activation energy, E_A of the metal.

$MTF = A(J^{-n})e^{Ea/kT}$

Since copper has higher activation energy than aluminum, it is more resistant to electromigration failures [3].

There are a few challenges associated with using copper for interconnects. Copper is difficult to etch using conventional etching techniques. Copper does not produce a volatile by-product during etching. For example, when chlorine gas is used to etch copper, it forms a chloride that does not readily evaporate. The chloride molecule sticks to the surface and prevents the underlying copper from etching. Another problem with copper is that it quickly diffuses into oxides and silicon, thereby causing junction spiking and shorts. Unlike aluminum, copper quickly oxidizes in air and does not form a protective oxide layer. Thus copper is less resistive to corrosion/oxidation.

In order to address these challenges, IBM introduced a unique additive processing technique to form copper IC interconnects, commonly known as Damascene process. The name Damascene originates in Damascus, the capital of modern Syria. Damascene process is reminiscent of the metal inlay techniques used in the Middle East since the middle ages [2].

In Damascene process, copper is planarized, using Chemical Mechanical Planaraztion technique, rather than being etched. Secondly in order to prevent copper contamination into oxide or silicon, a barrier layer is deposited before copper deposition. Typically, Tantalum, Tantalum nitride, or Titanium Nitride is used as barrier layer.

The Damascene process is an additive process. Firstly, the dielectric is deposited, and then dielectric is etched according to the defined photoresist pattern. Next, a barrier layer is deposited to prevent junction spiking. After that a thin seed layer of copper is deposited conformally over the surface. The seed layer is important, because without the seed layer the copper cannot be electrochemically deposited. After depositing

the seed layer, the structure is electroplated with copper. Final step is to planarize the excess copper. The process steps are shown in figure 1 below:

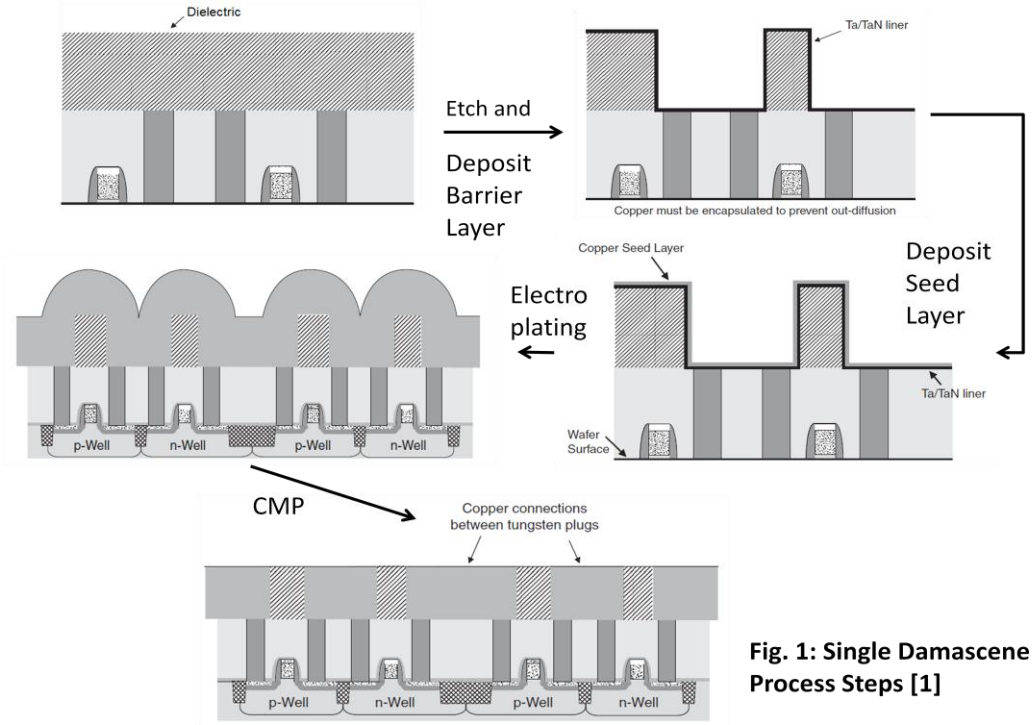

Fig. 1: Single Damascene Process Steps [1]

A variation of Damascene process is Dual Damascene process. In this process, the vias and the metal lines are created by etching holes and trenches in the dielectric, after which copper is deposited in a single step. In Dual Damascene process, one photo/etch step is needed for making holes for vias in the dielectric and another photo/etch step is needed for making trenches for metal lines. These two photo/etch steps can be performed in any order, i.e. via first then trench or trench first then via. The process steps are shown in figure 2 below:

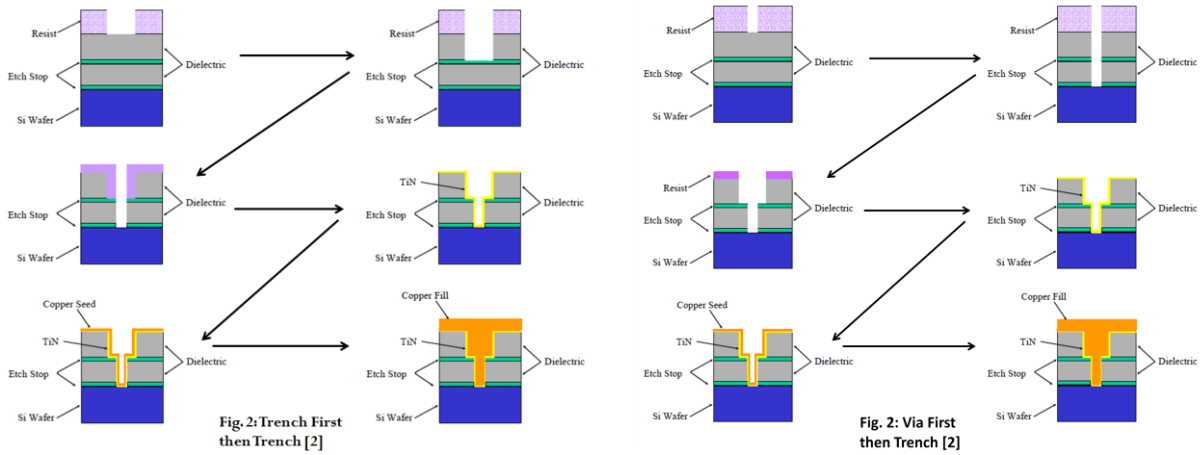

Fig. 2 : Dual Damascene Process [2]

Chemical Mechanical Planarization (CMP) is "a process of smoothing wafer surfaces with the combination of chemical and mechanical forces" [8]. The main reason for using a hybrid of chemical etching and free abrasive polishing is because mechanical grinding alone causes too much damage to the wafer surface, while chemical etching alone does not promote good planarization of surface. This process is generally used to remove silicon oxide, poly silicon, and metal surfaces and to provide plane surfaces.

There are several components involved in CMP. First, there is platen, which is a rotating base that holds all the components on top. Abrasive sponge-like pad covers platen and rotates with the platen to

mechanically polish the surface of wafer. Wafer carrier is composed of retaining ring, backing film, carrier housing, and back press vacuum. A wafer is held upside down by retaining ring on a backing film. The retaining ring keeps the wafer in correct horizontal position for even polishing. Both the pad and wafer carrier are then counter rotated while slurry containing both abrasives and reactive chemicals is passed underneath. The following figure illustrates the design of CMP.

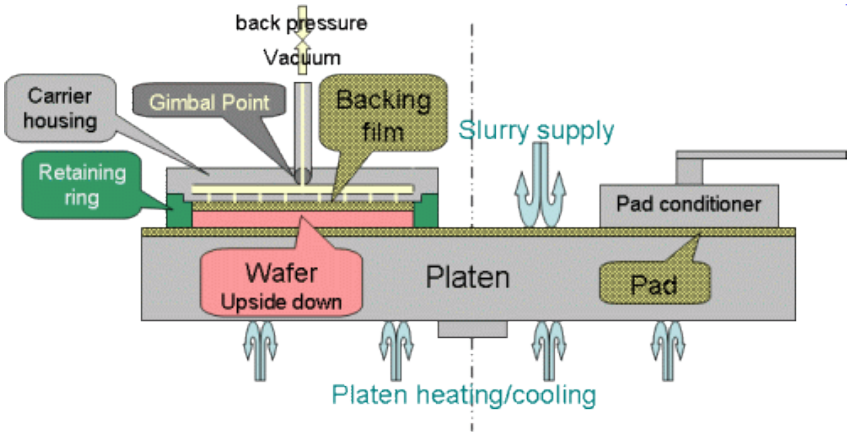

Figure 3 Illustration of Chemical Mechanical Planarization Machine [5].

CMP is achieved through applying load force provided by back press vacuum on the back of the wafer. When the pressure is applied on the wafer, the higher surfaces are polished away to level the surface layer. Also, most chemical reactions are isotropic and etch different crystal planes with different speed. CMP involves both chemical and mechanical effects at the same time. Some variables, such as temperature of the system, back pressure, velocity of the rotation, and slurry flow rate, play important roles in the quality of planarization. Typical process conditions are temperature from 10 °C to 70 °C, back pressure from 2 psi to 7 psi, velocity from 20 rpm to 80 rpm, and slurry flow rate from 100 mL/min to 200 mL/min. Typical removal rate for silicon oxide layer is approximately 2800Å/min and for metal is approximately 3500 Å/min.

The advantages of CMP are good selectivity, reduction of resist thickness variation, increased resolution of photolithographic process, improved step coverage of subsequent layer deposition, and multi-level interconnection. CMP encourages no lapping, which means that it will only polish the selected material and stop polishing at non-selective layer, whereas different planarization techniques may remove different materials at the same rate. Also, because CMP smoothes the surface layer, this accounts for reduction of resist thickness variation. Any higher surfaces are polished away to level the surface layer. CMP is essential for multi-layer chips. Neat planarization will improve step coverage of subsequent layer deposition, such as metal copper or aluminum, thus it maximizes the interconnection between the surface layers. This will promote multi-layer chips to be faster and more reliable because any bad connection between layers will be minimized. CMP also increases the resolution of photolithographic process by reducing the depth of focus. In order to project a photolithographic beam onto the surface of a wafer, the roughness of the surface of the wafer must be less than half of the depth of focus of the wafer. Smoothing the surface layer will reduce the depth of focus, therefore, improving the resolution of photolithography.

Nevertheless, there are some limitations seen by CMP. Dishing and erosion occurs due to local planarization in which some areas of the wafer polish faster than the others. Dishing results in a well-like shape. CMP is also subjected to stress cracking, scratching, and corrosive attacking from slurry chemicals. The wafer is very weak and thin; as a result, over pressuring the wafer will lead to stress cracking or scratching the surface of the wafer. CMP process is also time-consuming and expensive.

Works Cited

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