High Frequency Hybrid $\pi$ Model for BJT

What internal capacitances can we predict from the physical structure?

- **Forward active mode**: base-collector reverse biased, base-emitter forward biased
- Base-collector capacitance is depletion capacitance: $C_{\mu} \approx 1\text{-}5 \text{ pF}$
- Emitter-base capacitance has both depletion and diffusion components: $C_\pi \approx 5\text{-}50 \text{ pF}$
- $r_\mu$ typically neglected because $C_{\mu}$ is often more important

Cutoff Frequency: short circuit collector current gives limiting behavior that is not complicated by the external circuit:

$$i_c = \left( g_m - sC_{\mu} \right) v_\pi$$

$$v_\pi = i_b \left( r_\pi \left| \frac{1}{sC_\pi} \right| \frac{1}{sC_{\mu}} \right)$$

$$\beta_{ac} = h_{fe} = \frac{i_c}{i_b} = \frac{g_m - sC_{\mu}}{1 + \frac{1}{r_\pi} + s \left( C_\pi + C_{\mu} \right)} = \frac{g_m r_\pi}{1 + s r_\pi \left( C_\pi + C_{\mu} \right)}$$
Unity Gain Bandwidth for BJT

Common emitter current gain has a single pole response with 3dB frequency

\[ \omega_\beta = \frac{1}{r_\pi (C_\pi + C_\mu)} \]

and unity gain bandwidth (frequency at which gain drops to unity)

\[ \omega_T = g_m r_\pi \omega_\beta = \frac{g_m}{(C_\pi + C_\mu)} \]

\[ f_T = \frac{g_m}{2\pi (C_\pi + C_\mu)} \]

at low \( I_c \) \( f_T \propto g_m \propto I_c \) since capacitance dominated by depletion

at mid \( I_c \) capacitance dominated by \( C_\pi \) diffusion

at high \( I_c \) \( f_T \downarrow \) because \( h_f \downarrow \)
Fig. 5.67 (a) High-frequency equivalent circuit model for the MOSFET; (b) the equivalent circuit for the case the source is connected to the substrate (body); (c) the equivalent circuit model of (b) with $C_{db}$ neglected (to simplify analysis).
Unity Gain Bandwidth for MOS

What internal capacitances can we predict from the physical structure?

• Gate capacitance: parallel plate capacitor with channel, split between gate-to-source and gate-to-drain depending on mode of operation
• Overlap capacitance: source and drain diffusions extend slightly under gate oxide
• Junction capacitance: reverse biased junctions between source and drain diffusions and body

Cutoff Frequency: short circuit collector current gives limiting behavior that is not complicated by the external circuit

\[ i_o = (g_m - sC_{gd})v_{gs} \]

\[ v_{gs} = \frac{i_i}{s(C_{gs} + C_{gd})} \]

\[ \frac{i_o}{i_i} = \frac{g_m - sC_{gd}}{s(C_{gs} + C_{gd})} \approx \frac{g_m}{s(C_{gs} + C_{gd})} \]

Common source current gain drops to unity at the frequency (unity gain bandwidth)

\[ \omega_r = \frac{g_m}{(C_{gs} + C_{gd})} \]

\[ f_r = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \]
BJT and MOS Differential Pairs

Basic configuration:
two matched transistors joined at emitter and biased by constant current source

\[
\begin{align*}
v_{cm} &= \frac{v_1 + v_2}{2} \\
v_d &= v_1 - v_2
\end{align*}
\]

• Signal is composed of differential and common mode components
• With equal inputs, the constant current divides equally between the two transistors
• When one input is greater than the other, more current flows in that transistor
• With relatively small voltages we can steer the current from one side of the pair to the other
Fig. 6.2  Different modes of operation of the differential pair: (a) The differential pair with a common-mode input signal $v_{CM}$. (b) The differential pair with a “large” differential input signal. (c) The differential pair with a large input signal of polarity opposite to that in (b). (d) The differential pair with a small differential input signal $v_i$. 
Large Signal Operation of BJT Diff Pairs

\[ I_{E1} = \frac{I_S}{\alpha} e^{\frac{V_{B1}-V_T}{V_T}} \]

\[ I_{E2} = \frac{I_S}{\alpha} e^{\frac{V_{B2}-V_T}{V_T}} \]

\[ I_{E1} = e^{\frac{V_{B1}}{V_T}} \]

\[ I_{E2} = e^{\frac{V_{B2}}{V_T}} \]

\[ I = I_{E1} + I_{E2} = \frac{I_S}{\alpha} e^{-\frac{V_T}{V_T}} \left( e^{\frac{V_{B1}}{V_T}} + e^{\frac{V_{B2}}{V_T}} \right) \]

\[ I_{E1} = \frac{I_S}{\alpha} e^{\frac{V_{B1}}{V_T}} \]

\[ I_{E2} = \frac{I}{e^{\frac{V_{B2}}{V_T}} + e^{\frac{V_{B1}}{V_T}}} \]

\[ I_{C1} = \frac{\alpha I}{V_{B1}-V_T} \]

\[ I_{C2} = \frac{\alpha I}{V_{B2}-V_T} \]

- If the base voltages are equal, the current divides equally between the two transistors irrespective of the common mode voltage.
- A relatively small difference voltage will cause the current to flow almost entirely in one transistor.
Small Signal Operation of BJT Diff Pairs

Collector Currents

\[ v_d = v_{b1} - v_{b2} \]
\[ I_{c1} = \frac{\alpha I}{1 + e^{\frac{v_d}{V_T}}} \]
\[ I_{c2} = \frac{\alpha I}{1 + e^{\frac{v_d}{V_T}}} \]
\[ I_{c1} = \frac{\alpha I}{2} + \frac{\alpha I}{2} \frac{v_d}{2V_T} \]
\[ I_{c2} = \frac{\alpha I}{2} - \frac{\alpha I}{2} \frac{v_d}{2V_T} \]
\[ \Delta I = \frac{I_{c1} - I_{c2}}{2} = \frac{\alpha I}{2} \frac{v_d}{2V_T} = g_m \frac{v_d}{2} \]
\[ g_m = \frac{\alpha I}{2V_T} \]

For a BJT diff pair with resistive loads connected to the collectors, this leads to output voltages

\[ V_{c1} = \left( V_{cc} - \frac{\alpha I}{2} R_c \right) - g_m R_c \frac{v_d}{2} \]
\[ V_{c2} = \left( V_{cc} - \frac{\alpha I}{2} R_c \right) + g_m R_c \frac{v_d}{2} \]
Small Signal Operation of BJT Diff Pairs (cont’d.)

The input differential resistance is the resistance seen between the two bases. Using the resistance reflection rule:

\[ R_{id} = \frac{v_d}{i_b} = (\beta + 1) \frac{2r_e}{2r_e} = r_e \]

The output voltage can be taken differentially (between the two collectors), which gives a differential voltage gain:

\[ A_d = \frac{V_{C1} - V_{C2}}{V_d} = -g_m R_C \]

When the output voltage is taken single-endedly (from one of the collectors), then the voltage gain is given by:

\[ A_d = \frac{V_{C1}}{V_d} = -\frac{1}{2} g_m R_C \]

When we consider the small signal model, we find that the finite output resistance of the BJT transistor modifies the differential voltage gain:

\[ A_d = -g_m \left( R_C \parallel r_o \right) \]

When the output voltage is taken differentially, we find that common mode output voltage is zero and that the common gain is zero. (The circuit rejects common mode inputs.) However, when the output is taken single-endedly, the common mode gain is given by (where R is the incremental output resistance of the current source):

\[ A_{cm} = -\frac{\alpha R_C}{2R} \]

Which leads to a common mode rejection ratio (CMRR):

\[ CMRR = \left| \frac{A_d}{A_{cm}} \right| = \frac{g_m R}{\alpha} \text{ or (in dB) } 20 \log \frac{g_m R}{\alpha} \]
Large Signal Operation of MOS Diff Pairs

\[ I_{D1} = \frac{1}{2} k_n' \frac{W}{L} (V_{gs1} - V_{th})^2 \quad I_{D2} = \frac{1}{2} k_n' \frac{W}{L} (V_{gs2} - V_{th})^2 \]

\[ \sqrt{I_{D1}} = \sqrt{\frac{k_n' W}{2} \frac{L}{L}} \quad \sqrt{I_{D2}} = \sqrt{\frac{k_n' W}{2} \frac{L}{L}} \]

\[ v_d = V_{gs1} - V_{gs2} = \sqrt{I_{D1}} - \sqrt{I_{D2}} \]

\[ I = I_{D1} + I_{D2} \]

\[ I_{D1} = \frac{I}{2} + \sqrt{\frac{k_n' W}{L} I \left( \frac{v_d}{2} \right)^2 - 1} \]

\[ I_{D2} = \frac{I}{2} - \sqrt{\frac{k_n' W}{L} I \left( \frac{v_d}{2} \right)^2 - 1} \]

Let \[ \frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{th})^2 \]

\[ I_{D1} = \frac{I}{2} \left( \frac{I}{V_{GS} - V_{th}} \right) \left( \frac{v_d}{2} \right) \sqrt{1 - \left( \frac{v_d}{2 V_{GS} - V_{th}} \right)^2} \]

\[ I_{D2} = \frac{I}{2} \left( \frac{I}{V_{GS} - V_{th}} \right) \left( \frac{v_d}{2} \right) \sqrt{1 - \left( \frac{v_d}{2 V_{GS} - V_{th}} \right)^2} \]

\[ |v_d|_{max} = \sqrt{2} (V_{GS} - V_{th}) \]

\[ |v_d|_{max} = \sqrt{2} (V_{GS} - V_{th}) \]

- If the gate voltages are equal, the current divides equally between the two transistors
- A relatively small difference voltage will cause the current to flow almost entirely in one transistor
Small Signal Operation of MOS Diff Pairs

Drain Currents

\[
I_{D1} \approx \frac{I}{2} + \left( \frac{I}{V_{GS} - V_{th}} \right) \left( \frac{v_d}{2} \right)
\]

\[
I_{D2} \approx \frac{I}{2} - \left( \frac{I}{V_{GS} - V_{th}} \right) \left( \frac{v_d}{2} \right)
\]

\[
g_m = \frac{2I_D}{V_{GS} - V_{th}} = \frac{I}{V_{GS} - V_{th}}
\]

\[
I_{D1} = \frac{I}{2} + g_m \left( \frac{v_d}{2} \right) \quad I_{D2} = \frac{I}{2} - g_m \left( \frac{v_d}{2} \right)
\]

\[
I_{d} = g_m \left( \frac{v_d}{2} \right)
\]

\[
|v_d|_{\text{max}} = \sqrt{2} \left( V_{GS} - V_{th} \right)
\]

For a MOS diff pair with resistive load, this leads to output voltages

\[
V_{D1} = \left( V_{DD} - \frac{I}{2} R_D \right) - g_m R_D \frac{v_d}{2}
\]

\[
V_{D2} = \left( V_{DD} - \frac{I}{2} R_D \right) + g_m R_D \frac{v_d}{2}
\]
Small Signal Operation of MOS Diff Pairs (cont’d.)

The output voltage can be taken differentially (between the two drains), which gives a differential voltage gain:

\[ A_d = \frac{V_{D1} - V_{D2}}{v_d} = -g_m R_D \]

When the output voltage is taken single-endedly (from one of the drains), then the voltage gain is given by:

\[ A_d = \frac{V_{DL}}{v_d} = -\frac{1}{2} g_m R_D \]

When we consider the small signal model, we find that the finite output resistance of the MOS transistor modifies the differential voltage gain:

\[ A_d = -g_m \left( R_D \parallel r_o \right) \]

When the output voltage is taken differentially, we find that common mode output voltage is zero and that the common gain gain is zero. (The circuit rejects common mode inputs.) However, when the output is taken single-endedly, the common mode gain is given by (where \( R \) is the incremental output resistance of the current source):

\[ A_{cm} = -\frac{R_D}{2R} \]

Which leads to a common mode rejection ratio (CMRR):

\[ CMRR = \left| \frac{A_d}{A_{cm}} \right| = g_m R \text{ or (in dB) } 20 \log g_m R \]