A. Laboratory description

The purpose of this experiment is for us to observe and understand the current-voltage characteristics of MOSFETs, and learn how to design and build an amplifier with it. An amplifier can sense a voltage signal from the input port, and generate a larger signal at the output. The signal can be in the form of voltage, current, electron charge, etc. The most convenient way is to use the electrical potential, voltage.

Please refer to Chapter 4 for the characteristics of MOSFETs. First of all, the physical structure of a typical n-channel MOSFET is shown in Fig. 4.1.

![Diagram of n-channel MOSFET](image)

**Figure 4.1** Physical structure of the enhancement-type NMOS transistor: (a) perspective view; (b) cross-section. Typically $L = 0.1$ to 3 $\mu$m, $W = 0.2$ to 100 $\mu$m, and the thickness of the oxide layer ($t_{ox}$) is in the range of 2 to 50 nm.
In a MOSFET, there are four terminals: the source, the drain, the gate, and the substrate (body). The proper way to bias an n-MOSFET is shown in Fig. 4.3 below. In this specific case, the body is shorted to the source. With source (defined to be “the source of carriers”) grounded (or, actually, being shorted to the common potential), the gate is biased by $v_{GS}$, and $v_{DS}$ is applied to the drain. The leakage current through the gate is approximately zero, or negligible as far as we are concerned here in this experiment. The most popular way to present the electrical property of an nMOSFET is to show its “current versus voltage characteristics in the common-source configuration.” That is, the measured $i_D$ is shown versus the sweeping $v_{DS}$, as a function of a stepping $v_{GS}$.

One example is illustrated in Fig. 4.11. For this “enhancement-mode” n-MOSFET, the gate bias must be more positive than the threshold voltage $V_t$ (e.g., +2 Volt), in order to induce a conductive channel and thus a measurable $i_D$. Further, the more positive the gate voltage is, the higher the drain current. The threshold voltage $V_t$ is determined by the physical structure and for the thousands of MOSFETs on the same wafer, the measured standard deviation is about 2mV.
In the text, section 4.2.2, there are equations that you need to follow. The end result is that there are these two operation regimes, and the corresponding equations describing $i_D$ as a function of $v_{DS}$ and $v_{GS}$ are:

1. The “Diode region” is defined by $v_{DS} \leq (v_{GS} - V_t)$, and
   \[ i_D = k_n \frac{W}{L} \left( (v_{GS} - V_t) v_{DS} - \frac{1}{2} (v_{DS})^2 \right). \]

2. The “Saturation region” is defined by $v_{DS} \geq (v_{GS} - V_t)$, and
   \[ i_D = \frac{1}{2} k_n \frac{W}{L} (v_{GS} - V_t)^2. \]

These two equations are derived by some physical assumptions on the structure, doping profile, shape, material properties, transport mechanism, temperature, etc. By and large, they work well and can be used to predict the current within 10%.

The p-MOSFET is similar in structure, but now the conductive carriers are “holes,” or, vacancy of electrons. Section 4.2.4 describes the characteristics of the p-channel MOSFET. An example is shown in the figure below. (From http://homepages.cae.wisc.edu/~kursun.)

Notice that the source is defined to be “the source of carriers.” For p-MOS, in order to draw positive holes from the source to the drain, the drain-to-source bias should be negative. The gate-to-source bias should be more negative than the threshold voltage, for inducting holes at the channel. The threshold voltage for “enhancement-mode” pMOS is negative, for example, -2 Volt.

There are also two operation regimes and the corresponding equations describing $i_D$ as a function of $v_{DS}$ and $v_{GS}$ are:

3. The “Diode region” is defined by $v_{DS} \geq (v_{GS} - V_t)$, and
   \[ i_D = k_p \frac{W}{L} \left( (v_{GS} - V_t) v_{DS} - \frac{1}{2} (v_{DS})^2 \right). \]

4. The “Saturation region” is defined by $v_{DS} \leq (v_{GS} - V_t)$, and
   \[ i_D = \frac{1}{2} k_p \frac{W}{L} (v_{GS} - V_t)^2. \]
Note that the sign of drain current $i_D$ for pMOS is also positive. This is because of the convention defined in the textbook. See the circuit diagram taken from Fig. 4.18 below. The drain current for pMOS in this textbook is opposite to that defined for nMOS.

The most important application of transistors is in signal amplification. The amplifier to be built in this laboratory is a “single n-MOSFET amplifier wired in the common-source (CS) configuration.” For convenience here, the nMOSFET has its body contact shorted to the source. That is, the nMOSFET is treated as a three terminal device, including the gate, the source and the drain. The source terminal is shorted to the circuit common, and the signal to be amplified is sent in from the gate terminal, while the amplified output signal is taken out of the drain terminal. The circuit described in Fig. P4.77 (for problem 4.77), shown below, is a typical example. You will use this circuit and design the values of the resistors, so that the voltage gain is about $-10$. The small signal (therefore, it must be ac) voltage gain is defined to be:

$$\text{voltage gain} \equiv \frac{v_o}{v_{\text{sig}}}.$$
terminal of the MOSFET, there is a “bias capacitor” in parallel with the resistance of 3kΩ. This RC network at the source determines the frequency dependence of the voltage gain near dc.

**B. Pre-laboratory report**

1. Draw a circuit diagram, like this one below. Discuss how you would use the “load line” concept (like what you have used in lab#1) for measuring the I-V characteristics of an n-MOSFET.

   ![Circuit Diagram]

2. Similarly, use the same circuit and replace the nMOS by a pMOSFET. Discuss how you would use the “load line” concept (like what you have used in lab#1) for measuring the I-V characteristics of a p-MOSFET. Pay attention to the polarity of the bias and the direction of the current flow.

3. Use PSPICE to simulate the I-V characteristics of the n-MOSFET. Use the transistor array CA3600E (part number CA3600E) in your simulation. This IC is obsolete, but is equivalent to the newer HEF4007UB. Use a voltage ranges for the drain and the gate, such that the simulation result can show the span of I-V curves.

4. Tip: When doing PSPICE for this chip, short the unused terminal together, and keep them floating. Or, you have to observe that \( V_{DD} \) be more positive than \( V_{SS} \).

5. Do PSPICE simulation of an individual p-MOSFET. Use a voltage ranges for the drain and the gate, such that the simulation result can show the span of I-V curves.

6. What is the origin of the series resistance of a voltage source? What is the voltage source of the function generator that you have been using in our laboratory?

7. In the CS amplifier, what is the gate coupling capacitor for? Based on its function, what is the typical value? Explain why so.

8. What is the purpose of the capacitor connected in series with the output signal path? What is the typical value?

9. What is the purpose of the capacitor connected in between the transistor’s source terminal and common? What is the typical value?

10. Use the circuit diagram shown in Fig. P4.77 and determine the values of all resistors and all capacitors. The nMOSFET to be used is taken from the CMOS chip HEF4007UB. The key specifications are listed below.
   (i) the amplitude of the voltage gain is larger than 7, that is, \( |v_{sig}/v_o| > 7 \) (the larger, the better);
   (ii) the lower “3dB frequency” \( (f_L, \text{ see section 4.9.1}) \) is at most 100Hz (the lower, the better);
   (iii) the higher “3dB frequency” \( (f_H, \text{ see section 4.9.1}) \) is at least to 20kHz (the higher, the better).

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11. PSPICE simulate the CS amplifier, and obtain the simulated dc voltages and currents everywhere.

12. PSPICE simulate the frequency dependence of the voltage gain, which is defined to be the ratio $v_{\text{sig}} / v_o$. Plot the frequency dependence of both the amplitude and the phase. The amplitude plot would look like that shown in Fig. 4.49.

\[ \begin{align*}
\text{C. What to do in the laboratory} \\
\text{I. Measure the n-MOS characteristics} \\
\text{1. Wire up the circuit (using the same load line concept) and measure the characteristics of a n-MOSFET off the HEF4007UB chip.} \\
\text{2. For the n-MOS, tie the substrate terminal to the source terminal.} \\
\text{3. Record the data, that is, the current versus voltage characteristics in the common-source configuration.} \\
\text{4. Note that } V_{DS} = V_D - V_S, \text{ and } V_D \text{ is not the same as } V_{DD} \text{ at the output of the dc power supply. There is voltage drop across the load resistor } R_D. V_{DS} \text{ is measured by the digital voltmeter, across the Drain terminal and the Source terminal. Measure } V_{GS} \text{ to be sure that the Gate terminal has received the voltage from the dc voltage source } V_{GG}. \\
\text{5. Obtain the threshold voltages } V_t \text{ of the n-MOSFET. The method is to plot (your measured data) } i_D \text{ versus } v_{GS} \text{ at a fixed, small (dc) } V_{DS}. \text{ The dependence should be close to linear, when } V_{DS} \text{ is small (i.e., the MOS is operated in the linear region). Extrapolate the linear line to the } v_{GS} \text{ axis, where this linear line intersects with } v_{GS} \text{ is a measure of } V_t. \text{ The same } i_D \text{ versus } v_{GS} \text{ characteristic measured with a large } V_{DS} \text{ (while the MOS operates in the linear region).}
\end{align*} \]
saturation region) will be parabolic, as shown in Fig. 4.62. Do measurement of $V_t$ by either method.

**Figure 4.62** Sketches of the $I_D=I_{DS}$ characteristics for MOSFETs of enhancement and depletion types, of both polarities (operating in saturation). Note that the characteristic curves intersect the $V_{GD}$ axis at $V_t$. Also note that for generality somewhat different values of $|V_t|$ are shown for n-channel and p-channel devices.

II. Measure p-MOS characteristics

1. Measure the characteristics of a p-MOSFET off the HEF4007UB chip. For the p-MOS, tie the substrate terminal to the $V_{DD}$ terminal.
2. Record the data.
3. Obtain the threshold voltage of the p-MOSFET, by using an approach identical to that discussed in I.4 above for n-MOS.

III. Connect up the CS amplifier using a single nMOSFET according to your circuit diagram.

1. Increase $V_{DD}$ from zero up to your designed value.
2. Measure the dc voltages at all nodes and determine where the operating point is at this moment. Is this the same as what you expected? If yes, proceed. If not, then troubleshoot. Be certain that the MOSFET works in the operation condition that is very close to what you have designed. Record the voltages and currents under this dc condition.
3. Obtain a small signal, e.g., 10 mV, from the function generator as the $v_{sig}$. You can use a voltage divider to reduce the output voltage. For example, the signal generator outputs 1V, and you wire up a 1000ohm:10ohm voltage divider and you will obtain approximately 10mV. Our typical resistor in the laboratory has a tolerance of a few percent.
4. Measure the ac voltage gain ($v_o/v_{sig}$). Compare this measured value with your calculated one. Since the oscilloscope has two channels, display the input voltage on one channel and the output on the other. Dump this data and have a hardcopy for your post-lab report.
5. Record the frequency dependence of the voltage gain. Find the “3dB” frequencies, $f_{hi}$ and $f_{li}$.
6. Record the frequency dependence of the phase change between the input and output. That is, the input signal is the reference.

**D. Post laboratory report**

1. Report your circuit and data. Discuss the operation of your circuit, specifically, whether the measured data is approximately the same as your PSPICE simulation. If not, explain why.
2. Discuss what factors determine the frequency dependence of the gain and phase shift. That is to say, what else you can do to further enhance the voltage gain, lower the $f_L$, and increase the $f_H$. 