

ENEE 244 (01**). Spring 2006

Homework 6

Due back in class on Wednesday, May 10.

- Design a modulo-6 counter, which counts 0,1,2,3,4,5,0,1,..... The counter counts the clock pulses if its enable input, w , is equal to 1. Use D flip flops in your circuit. If the circuit ever finds itself in an unused state (6 or 7), it should transition to state 0 with the next clock trigger to avoid being stuck in an unused state. Use a formal design procedure. No credit for doing an intuitive design!

Drawing the state table for the given modulo 6 counter.

Present state			Input	Next state		
Q2	Q1	Q0	W	Q2+	Q1+	Q0+
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	1	0	0
1	0	0	1	1	0	1
1	0	1	0	1	0	1
1	0	1	1	0	0	0
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	0	0
1	1	1	1	0	0	0

For D flip-flops, the input into the flip flops is the same as the next state that are shown in the table. ($D_2=Q_{2+}$, $D_1 = Q_{1+}$, $D_0 = Q_{0+}$).

Now drawing 4-variable K maps for D flip flop inputs D_2 , D_1 and D_0 we get the following result (K-maps not shown):

$$D_2 = Q_2Q_1'Q_0' + Q_2Q_1'W' + Q_2'Q_1Q_0W$$

$$D_1 = Q_2'Q_1Q_0' + Q_2'Q_1W' + Q_2'Q_1'Q_0W$$

$$D_0 = Q_2'Q_0'W + Q_1'Q_0'W + Q_2'Q_0W' + Q_1'Q_0W'$$

The above equations completely define the required circuit.

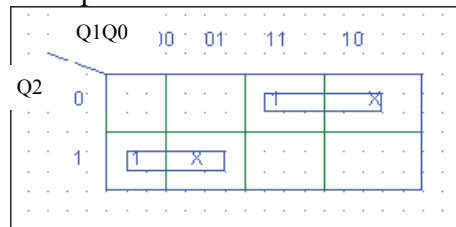
- Design a counter with T flip flops that goes through the following binary repeated sequence 0,1,3,7,6,4. Show that when the states 010 and 101 are considered as don't care conditions the counter may not operate properly.

There are $\text{ceiling}(\log_2 6) = 3$ flip-flops required.
 Drawing the state table:

Present state			Next state			Excitation		
Q2	Q1	Q0	Q2+	Q1+	Q0+	T2	T1	T0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	X	X	X	X	X	X
0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	0
1	0	1	X	X	X	X	X	X
1	1	0	1	0	0	0	1	0
1	1	1	1	1	0	0	0	1

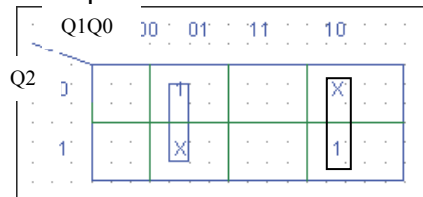
Drawing the K maps for T2, T1 and T0:

K map for T2



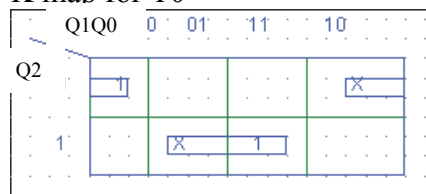
$$T2 = Q2Q1' + Q2'Q1$$

K map for T1



$$T1 = Q1Q0' + Q1'Q0$$

K map for T0



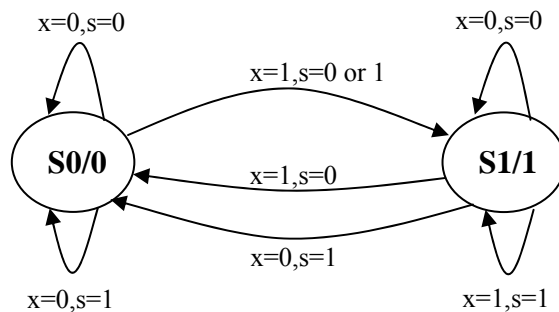
$$T0 = Q2Q0 + Q2'Q0'$$

In the K-maps, all the don't cares were assigned to 1 in our choice, so the flip-flops will all toggle in states 010 and 101. Thus if the counter finds itself in state 010, it will transition to 101, and vice versa. This constitutes an infinite cycle of unused states. Hence the counter is **not** self-correcting -- if the counter ever finds itself in an unused state, it will remain in unused states forever.

3. Design a circuit that is a serial even parity generator. The circuit has two bits of input x and s , where x is the data input and s is the start. The input number is applied bit-by-bit to the x input. The start signal s is supposed to be set to 1 by the user to indicate the start of a new number. The new number's first bit is applied *at the same time* as $s=1$. A signal $s=0$ implies that the old number is continuing and x is the next bit of the old number. There is one output bit p which outputs the even parity bit of the number seen so far beginning from the cycle of the most-recently seen $s=1$ signal. In this way, this circuit can be used to compute the even parity of numbers of any length desired by the user. At startup, until the first $s=1$ is seen, the output is undefined. Design a Moore machine using JK flip-flops. Use a formal design procedure. Draw the resulting circuit. Recall that an even parity bit is such a bit that makes the number of 1s in the number seen so far, including the parity bit, to be even (i.e., the number of bits in the number seen so far is odd).

The state needs to keep track only of whether the number of 1s seen since the last $s=1$ is even or odd; hence only two states are needed. State S_0 outputs $p=0$ (number of 1s seen so far is even). State S_1 outputs $p=1$ (number of 1s seen so far is odd). The start state is S_0 .

State diagram:



Number of flip-flops: ceiling ($\log_2 2$) = 1.

Let that single flip-flop have inputs J, K and output Q .

State assignment: $S_0 \equiv (Q = 0)$; $S_1 \equiv (Q = 1)$.

No separate circuit is needed for the output since $p=Q$.

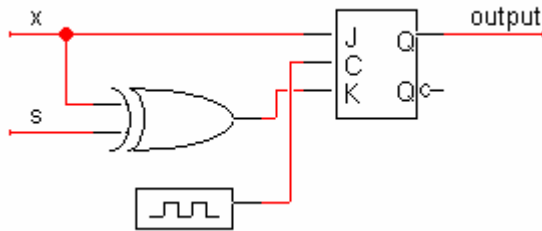
From this we can make a state table and excitation table:

Present state	Inputs		Next state	Excitation	
	x	s		Q^+	J
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	X
0	1	1	1	1	X
1	0	0	1	X	0
1	0	1	0	X	1
1	1	0	0	X	1
1	1	1	1	X	0

Next, 3-variable K-maps (not shown) are used to derive J,K in terms of Q, x, s.
This yields:

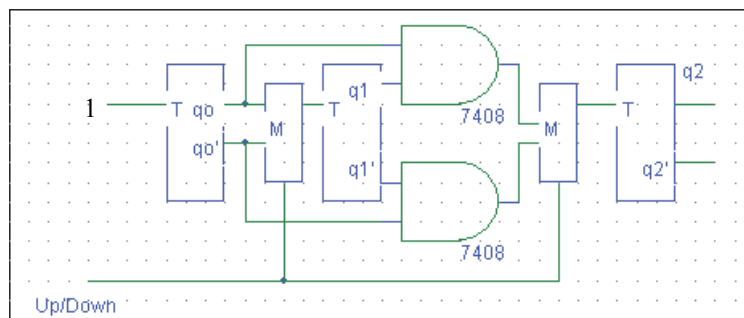
$$J = x$$

$$K = x's + xs'$$



- Design a three-bit up/down counter using T flip flops. It should include a control input called Up/Down. If Up/Down = 0, then the circuit behaves as an up counter. If Up/Down = 1, then the circuit should behave as a down counter. Do not use a formal design procedure; instead use your intuition or a variant of a design in the book.

For designing a 3 bit Up/Down counter we use 3 T flip flops and two 2 x 1 MUX
The design is as shown below.



In the diagram above the following are the symbols used:

T : T flip flop

M: 2 x 1 multiplexer

7408: AND gate

The T flip flops are triggered by the same clock, which is not shown. The intuition is that the least significant (leftmost) bit toggles in every cycle, but for higher bits, they toggle when all the bits that are less significant are either all one (up counter) or all zero (down counter). The MUXs are used select between these two possibilities.

- Design a 4-bit binary synchronous counter with D flip flops. Use an intuitive design procedure or a variant of a circuit in the book.

Refer to figure 6.33 of the Givone textbook. We see that a 4 bit synchronous circuit has been implemented using T flip-flops. Now we need to convert these T flip flops to D flip flops. We know that if the input to a T flip flop is T then if we need to use a D flip flop instead the input to the D flip flop must be $D = Q \oplus T$. This follows from how a T flip-flop is built from a D flip-flop in figure 6.23 earlier in the text.

The circuit given in the book in terms of FF equations is:

$$T_0 = E$$

$$T_1 = Q_0.E$$

$$T_2 = Q_0.Q_1.E$$

$$T_3 = Q_0.Q_1.Q_2.E$$

where E is the Count enable input.

So the inputs to the D flip-flop should be

$$D_0 = Q_0 \oplus E$$

$$D_1 = Q_1 \oplus (Q_0.E)$$

$$D_2 = Q_2 \oplus (Q_0.Q_1.E)$$

$$D_3 = Q_3 \oplus (Q_0.Q_1.Q_2.E)$$

The above equations completely specify the required counter with D flip-flops.