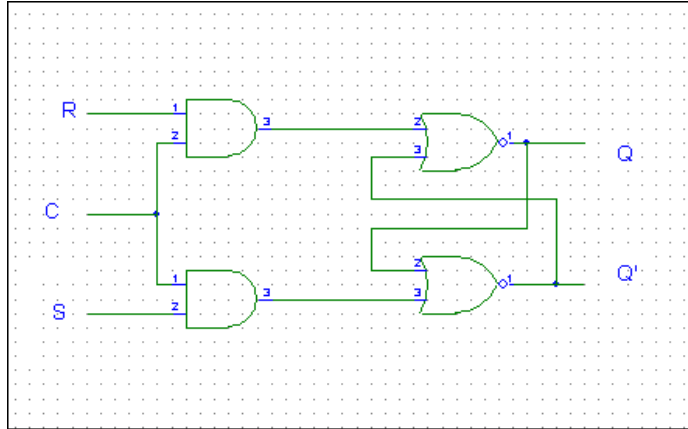


# ENEE 244 (01\*\*). Spring 2006

## Homework 5

*Due back in class on Friday, April 28.*

- Fill up the function table (truth table) for the following latch. How is this latch related to those described in the lectures and in the textbook? (Describe similarities and differences with the most closely related latch).



C	S	R	Q+	Q+'
0	X	X	Q	Q'
1	0	0	Q	Q'
1	0	1	0	1
1	1	0	1	0
1	1	1	0*	0*

The last row should not be used since it causes unpredictable behavior thereafter. We observe that this function table is identical to that of a gated SR latch.

- The gated S-R latch in Question 9 has unpredictable behavior if the S and R inputs are both equal to 1 when C changes to 0. One way to solve this problem is to create a *set-dominated* gated SR latch in which the condition S=R=1 causes the latch to be set to 1. Design a set-dominated gated SR latch. Show the circuit. (**Hint:** Let the original circuit remain as it is, but add some external circuitry.)

Since we want the latch to be Set-Dominated, it means that whenever R=S=1, the condition for Setting the latch should come about. Let us assume the external circuit takes the inputs S and R. Further the internal SR latch takes inputs Sint and Rint. The relation between S, R and Sint, Rint is given by the following truth table:

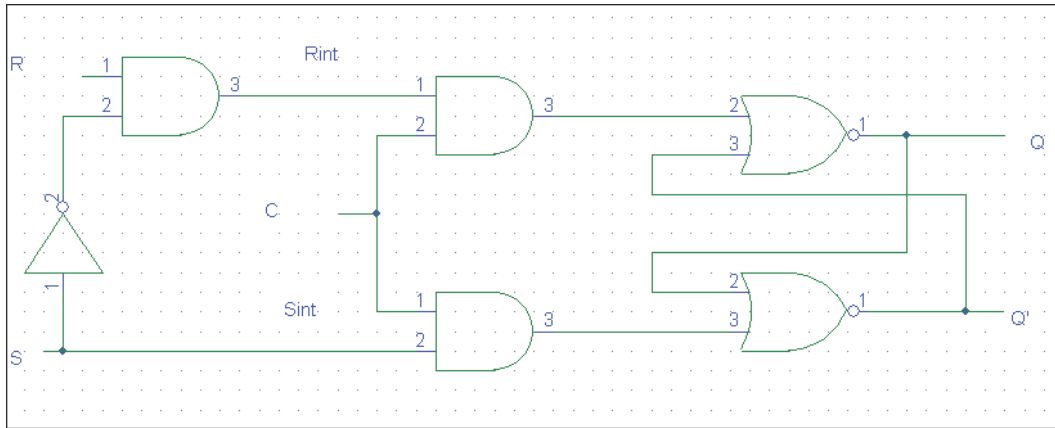
S	R	Sint	Rint
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	0

From the table,

$$S_{int} = SR' + SR = S$$

$$R_{int} = S'R$$

Thus the circuit is:



3. A PN flip-flop has 4 operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00,01,10, and 11, respectively. Tabulate its characteristic table (called the simplified function table by the Givone text). Derive its characteristic equation.

Characteristic table:

P	N	Q+
0	0	0
0	1	Q
1	0	Q'
1	1	1

Expanding this to a next-state table:

P	N	Q	Q+
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

By expressing the Q+ function as a canonical form function and minimizing using a K-map (not shown) we get:

$$Q+ = PQ' + NQ$$

4. Show how to implement a D flip-flop starting with a J-K flip-flop.

Here is the desired relationship between the external D input and the internal J,K inputs:

D	J	K
0	0	1 //This row is chosen to reset the JK FF
1	1	0 //This row is chosen to set the JK FF

Expressing J,K in terms of D:

$$J=D$$

$$K=D'$$

Thus to get a D flip flop from a JK FF, connect the D input to J and D' to K.

5. A sequential circuit contains two flip-flops T1 and T2. The circuit has no external inputs. The only external output are the values of the current state (Q1 and Q2). The flip-flop inputs are connected as:

$$T1 = Q1 + Q2$$

$$T2 = Q1' + Q2$$

Explain the function that the circuit performs.

The characteristic equation of a T FF is given by:

$$Q+ = T \oplus Q$$

We derive the transition equations of the circuit by substituting the FF input equations into the characteristic equation. This gives:

$$Q1+ = (Q1 + Q2) \oplus Q1$$

$$Q2+ = (Q1' + Q2) \oplus Q2$$

From this, we derive the transition table:

Present state (Q1Q2)	Next state (Q1+Q2+)
00	01
01	10
10	00
11	00

From the transition table, we can reason about the circuit. The circuit is a counter, i.e, a circuit that counts the number of clock pulses it gets. In particular it is a modulo-3 counter, which is a circuit that counts in the sequence 0,1,2, 0,1,2 .... Further it has the nice property such that if it ever enters the unused state of 3 (11) such as at startup, it returns to 0, never to go to state 3 again.

6. A sequential circuit has two JK flip-flops with outputs Q1 and Q2 and one input x. The circuit is described by the following flip-flop input equations:

$$J1 = x$$

$$J2 = x$$

$$K1 = Q2'$$

$$K2 = Q1$$

- Derive the next-state equations for the circuit.
- Draw the state diagram.

The characteristic equation of a JK FF is:

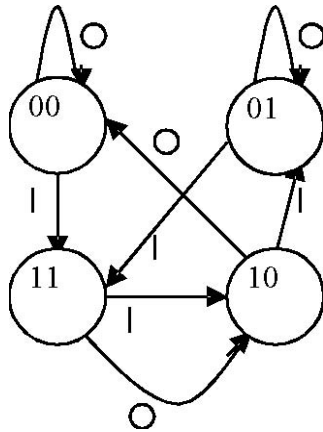
$$Q+ = JQ' + K'Q$$

Substituting the FF input formulas in the characteristic equation, we get:

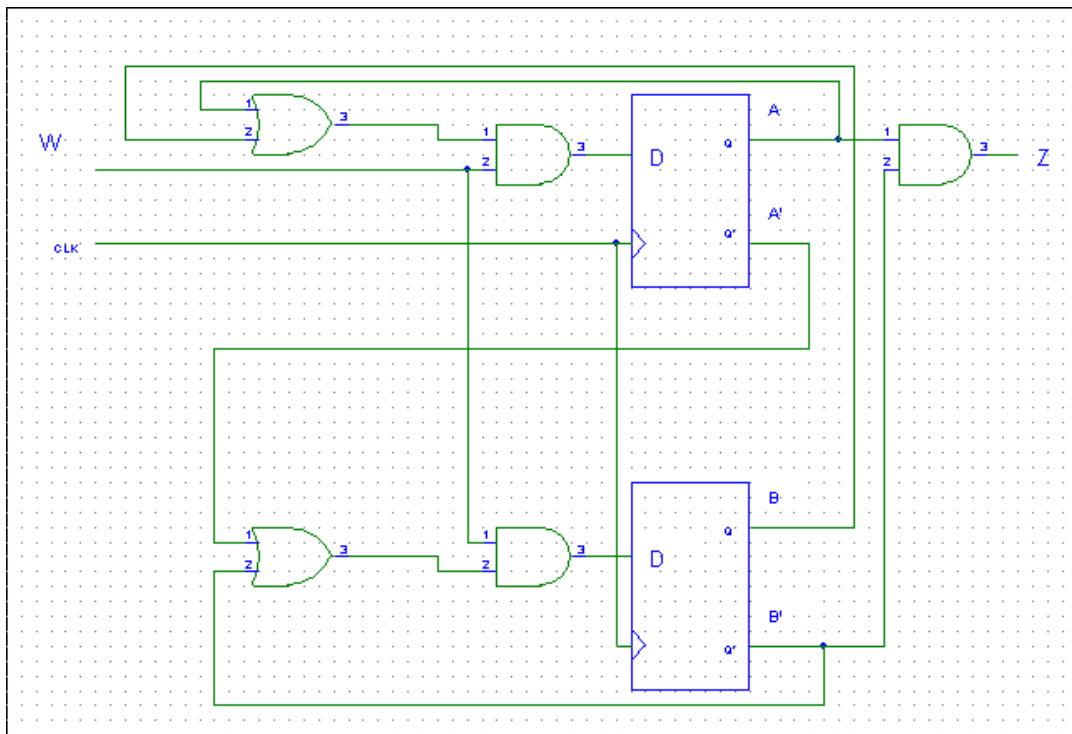
$$Q1+ = J1Q1' + K1'Q1 = xQ1' + Q2Q1$$

$$Q2+ = J2Q2' + K2'Q2 = xQ2' + Q1'Q2$$

From this, we can fill the state table (not shown) and from that, the state diagram:



7. Derive the state table for the circuit drawn below.



Here the FF inputs are:

$$DA = (QA + QB)W$$

$$DB = (QA' + QB')W$$

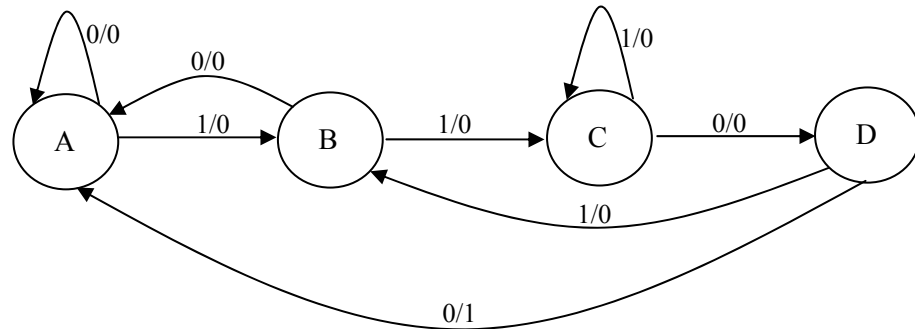
For a D FF, the FF inputs are equal to the next state. Thus the state table is:

PRESENT STATE BA	NEXT STATE W=0 BA	NEXT STATE W=1 BA	OUTPUT Z
00	00	10	0
01	00	11	1
10	00	11	0
11	00	01	0

8. Draw the state diagram for a Mealy machine that accepts an infinite sequence of bits, and outputs a 1 if the last four bits input are 1100; otherwise the output is 0. For example, for the input below, the output should be as shown:

INPUT: 00110110011.....  
 OUTPUT:00000000100....

Use no more than 4 states in your state diagram. Be careful that your solution works for the above input. What is the minimum number of flip flops needed for implementing your state diagram?



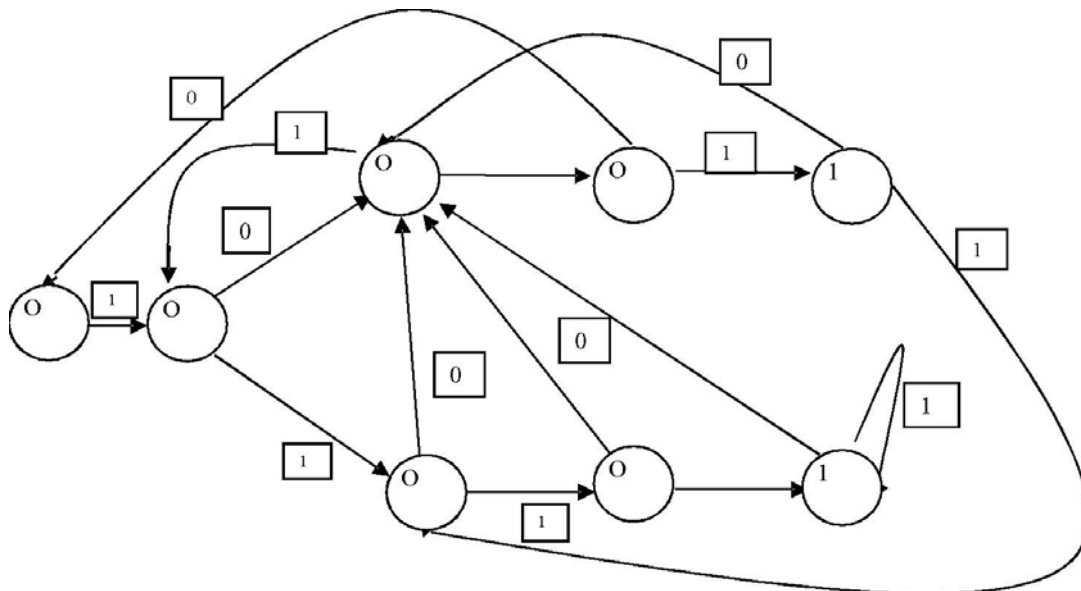
Note that this circuit requires four states. A Moore machine to implement the same circuit requires five states.

A four state machine can be implemented in  $\lceil \log_2 4 \rceil = 2$  flip-flops. //The  $\lceil x \rceil$  notation represents the ceiling of real number  $x$ .

9. Derive the state diagram for a Moore machine that has an input  $w$  and an output  $z$ . The machine has to generate  $z=1$  when the pervious four values of  $w$  were 1001 or 1111; otherwise the output  $z=0$ . Overlapping input patterns are allowed. Example:

w: 010111100110011111.....  
 z: 000000100100010011...

Use no more than eight states in your solution. What is the minimum number of flip flops needed for implementing your state diagram?



There are 8 states. The number of flip-flops is given by  $\log_2(k)$ , where  $k$ =number of states. Hence for 8 states, the number of flip-flops is  $\log_2(8) = 3$