

ENEE 244 (01**). Spring 2006

Homework 4

Due back in class on Friday, April 7.

1. Implement the following Boolean expression with exclusive-OR and AND gates only:
 $F = AB'CD' + A'BCD' + AB'C'D + A'BC'D.$
2. Determine whether the gate set {AND, EXCLUSIVE-OR} is functionally complete. Prove your answer.
3. A two-level all-NAND implementation of a complex logic function $z(x_1, x_2, \dots, x_n)$ has been fabricated in a IC at considerable expense. As the IC is about to be installed in a system it is discovered that all the gates it contains are actually NORs instead of NANDs. It is now too late to fix the IC itself, but it is possible to add some extra logic to the IC's input/output lines. So what should the IC designer do to fix this flaw so that the IC in question can be used?
4. Design a 4 bit combinational circuit 2's completer for an input $x = x_3x_2x_1x_0$. (The output generates the 2's complement of the input binary number) Show that the circuit can be constructed using exclusive-OR and AND gates only. Do not use any full adders.
5. A combinational circuit has 3 outputs F1, F2 and F3:
$$F1 = x'y'z' + xz$$
$$F2 = x y'z' + x'y$$
$$F3 = x'y'z + xy$$

Design the circuit with a decoder and external gates.

6. Demonstrate how to implement a 6:64 decoder using generic 2:4 and 4:16 decoders. The input decoders have enable inputs.
7. A majority function F takes three 1-bit inputs a,b and c, and produces a single bit as output that is one if and only if two or more bits of the input are one. Design this circuit using an 8:1 multiplexor.
8. The outputs of a 3-to-8 decoder are connected in order to the inputs of an 8-to-1 MUX. The inputs of the decoder are a,b and c; the select inputs of the MUX are d,e and f. What function does the 1-bit output of the MUX implement in terms of a,b,c,d,e and f?