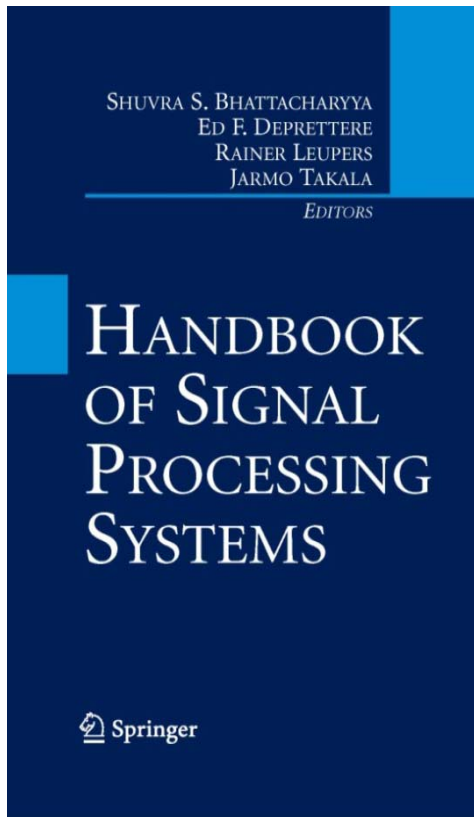


Handbook of Signal Processing Systems

Shuvra S. Bhattacharyya, Ed F. Deprettere, Rainer Leupers,
and Jarmo Takala, eds.



Handbook of Signal Processing Systems provides a standalone, complete reference to signal processing systems organized in four parts. The first part motivates representative applications that drive and apply state-of-the-art methods for design and implementation of signal processing systems; the second part discusses architectures for implementing these applications; the third part focuses on compilers and simulation tools; and the fourth part describes models of computation and their associated design tools and methodologies. Each part has 6-12 chapters from leading experts. A preliminary outline of chapter topics is listed below for each part.

Topics Covered:

Foreword by S. Y. Kung

1. Applications (Managing Editor : Shuvra Bhattacharyya)

- (1) *Signal Processing for Control* by William S. Levine
- (2) *Digital Signal Processing in Home Entertainment* by Konstantinos Konstantinides
- (3) *MPEG Reconfigurable Video Coding* by Marco Mattavelli, Jörn W. Janneck, and Mickaël Raulet
- (4) *Signal Processing for High-Speed Links* by Naresh Shanbhag, Andrew Singer, and Hyeon-min Bae
- (5) *Video Compression* by Yu-Han Chen and Liang-Gee Chen
- (6) *Low-power Wireless Sensor Network Platforms* by Jukka Suhonen, Mikko Kohvakka, Ville Kaseva, Timo D. Hämmäläinen, and Marko Hännikäinen
- (7) *Signal Processing for Cryptography and Security Applications* by Miroslav Knežević, Lejla Batina, Elke De Mulder, Junfeng Fan, Benedikt Gierlich, Yong Ki Lee, Roel Maes, and Ingrid Verbauwhede
- (8) *High-Energy Physics* by Anthony Gregerson, Michael J. Schulte, and Katherine Compton
- (9) *Medical Image Processing* by Raj Shekhar, Vivek Walimbe, and William Plishker
- (10) *Signal Processing for Audio HCI* by Dmitry N. Zotkin and Ramani Duraiswami
- (11) *Distributed Smart Cameras and Distributed Computer Vision* by Marilyn Wolf and Jason Schlessman

2. Architectures (Managing Editor : Jarmo Takala)

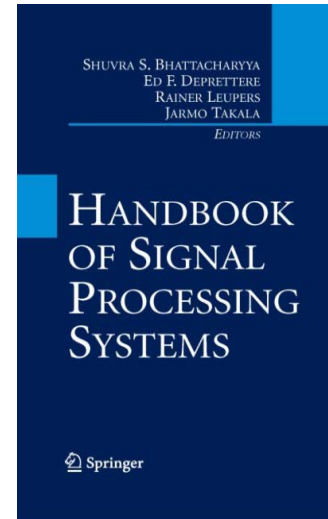
- (1) *Arithmetic* by Oscar Gustafsson and Lars Wanhammar
- (2) *Application-Specific Accelerators for Communications* by Yang Sun, Kiarash Amiri, Michael Brogioli, and Joseph R. Cavallaro
- (3) *FPGA-based DSP* by John McAllister
- (4) *General-Purpose DSP Processors* by Jarmo Takala
- (5) *Application Specific Instruction Set DSP Processors* by Dake Liu
- (6) *Coarse-Grained Reconfigurable Array Architectures* by Bjorn De Sutter, Praveen Raghavan, and Andy Lambrechts
- (7) *Multi-core System-on Chip* by Luigi Carro and Mateus Beck Rutzig
- (8) *DSP Systems using Three-Dimensional (3D) Integration Technology* by Tong Zhang, Yangyang Pan, and Yiran Li
- (9) *Mixed Signal Techniques* by Olli Vainio

3. Programming and Simulation Tools (Managing Editor : Rainer Leupers)

- (1) *C Compilers and Code Optimization for DSPs* by Björn Franke
- (2) *Compiling for VLIW DSPs* by Christoph W. Kessler
- (3) *Software Compilation Techniques for MPSoCs* by Rainer Leupers, Weihua Sheng, and Jeronimo Castrillon
- (4) *DSP Instruction Set Simulation* by Florian Brandner, Nigel Horspool, and Andreas Krall
- (5) *Optimization of Number Representations* by Wonyong Sung
- (6) *Intermediate Representations for Simulation and Implementation* by Jerker Bengtsson
- (7) *Embedded C for Digital Signal Processing* by Bryan E. Olivier

4. Design Methods (Managing Editor : Ed F. Deprettere)

- (1) *Signal Flow Graphs and Data Flow Graphs* by Keshab K. Parhi and Yanni Chen
- (2) *Systolic Arrays* by Yu Hen Hu and S.-Y. Kung
- (3) *Decidable Signal Processing Dataflow Graphs: Synchronous and Cyclo-Static Dataflow Graphs* by Soonhoi Ha and Hyunok Oh
- (4) *Mapping Decidable Signal Processing Graphs into FPGA Implementations* by Roger Woods
- (5) *Dynamic and Multidimensional Dataflow Graphs* by Shuvra S. Bhattacharyya, Ed F. Deprettere, and Joachim Keinert
- (6) *Polyhedral Process Networks* by Sven Verdoolaege
- (7) *Kahn Process Networks and a Reactive Extension* by Marc Geilen and Twan Basten
- (8) *Methods and Tools for Mapping Process Networks Onto Multi-Processor Systems-On-Chip* by Iuliana Bacivarov, Wolfgang Haid, Kai Huang, and Lothar Thiele
- (9) *Integrated Modeling using Finite State Machines and Dataflow Graphs* by Joachim Falk, Joachim Keinert, Christian Haubelt, Jürgen Teich, and Christian Zebelein



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