An Analog-to-Information converter for Biomedical Signals based on Compressive Sensing

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***Abstract*—In this paper an Analog-to-Information converter based on the Compressive Sensing (CS) paradigm and particularly suited for biomedical signals with Nyquist frequency up to 100 kHz is presented. The circuit has been designed and fabricated in CMOS 180 *nm* technology and exploits a 16-channel Random Modulation pre-Integration (RMPI) architecture, that has been proven to be the most versatile CS approach. The circuits also embeds a smart and innovative saturation checking mechanism, that allows signal reconstruction without performance reduction even in presence of saturation. Measurements on real electrocardiogram (ECG) and electromyogram (EMG) signals available in public databases confirm that circuit performances on different settings are aligned with the theoretical expected ones.**

***Index Terms*—Compressive Sensing, Analog-to-Information Converter (AIC), Rakeness, Biomedical signals, Smart saturation checking.**

I. Introduction

IN RECENT years, some application-specific Analog-to-Information Converters (AICs) have been proposed, exploiting input signal statistical features to reduce the amount of resources (hardware, time, energy, etc.) required per conversion with respect to standard and general purpose Nyquist-rate Analog-to-Digital converters (ADCs).

In this paper we consider AICs based on the paradigm of *Compressive Sensing* (CS) [1], [2], [3], [4], that aim at the acquisition of a signal with a smaller number of measurements with respect to what required by ADCs based on the classical Nyquist theory [5]. In particular, CS theory links the number of required measurements with the *actual information* of the signal independently on its *bandwidth*. To this aim, CS exploits the statistical feature known as *sparsity*, that indicates that the signal of interest can be expressed as the linear combination of only a few vectors of a given basis.

Under these assumption, the input signal can be compressed in way similar to that of common digital compression algorithms as shown in Fig. 1. In the standard digital compression approach of case (a) the input signal is first sampled and converted into digital words at Nyquist rate, then a proper DSP or finite-state machine ensures data compression by means on any lossless or lossy compression algorithm. The process is useful to save memory or energy in, respectively, data storage or transmission. The original signal can be easily restored by means of the proper decompression algorithm.

In the CS approach of Fig. 1(b), the analog input signal is first processed by a proper analog front-end (the CS encoder), that generates a small number of measurements that are sampled and converted by an ADC at a rate much smaller with respect to Nyquist one. The input signal is then recovered (we say *reconstructed*) by means of a proper decoder algorithm.

The main difference between the two approaches is that, in the large majority of cases, in (a) the compression algorithm is the one with the highest complexity (and so with the need for a more complex hardware and higher energy requirements), while decompression is usually much simpler. On the contrary, in (b) the CS encoder is based on a very simple and extremely low-power hardware, while complexity and power requirements are transferred to the decoding machine. As a consequence, while (a) is preferred when a single compression unit is used by many receivers, (b) finds a natural application when multiple encoders communicate with a single data aggregator. This is the case, for example, of a wireless body area network for medical telemetry [6], where a heterogeneous set of high energy efficiency, small form factor bio-sensor nodes transmit data to a single monitoring station [7]. Performance in this scenario are boosted since all biomedical signals present sparsity properties, allowing the CS approach to get a very high compression gains [8], [9], [10].

In this paper, we present an integrated AIC specifically designed for biomedical signals with CS capabilities. The circuit has been designed and fabricated in $180\,\mathrm{nm}$ CMOS technology and it is based on a 16-channel Random Modulation pre-Integration (RMPI) architecture [4]. The converter accepts an input signal with Nyquist frequency ranging from fractions of Hz to a hundred kHz, with a power consumption of about $27\,\mu\mathrm{W}$ per channel. The circuit also includes a shared 11-bit Successive Approximation Register (SAR) based ADC.

The most innovative feature with respect to any AIC already appeared in the literature [11], [12], [13] is that the presented prototype implements the smart saturation checking strategy proposed in [14]. Measurement results on artificially created test signals and on real signals point out that with the proposed approach it is possible to correctly reconstruct the input signal without any performance loss even in presence of a *weak* saturation, i.e., when the input signal amplitude is slightly

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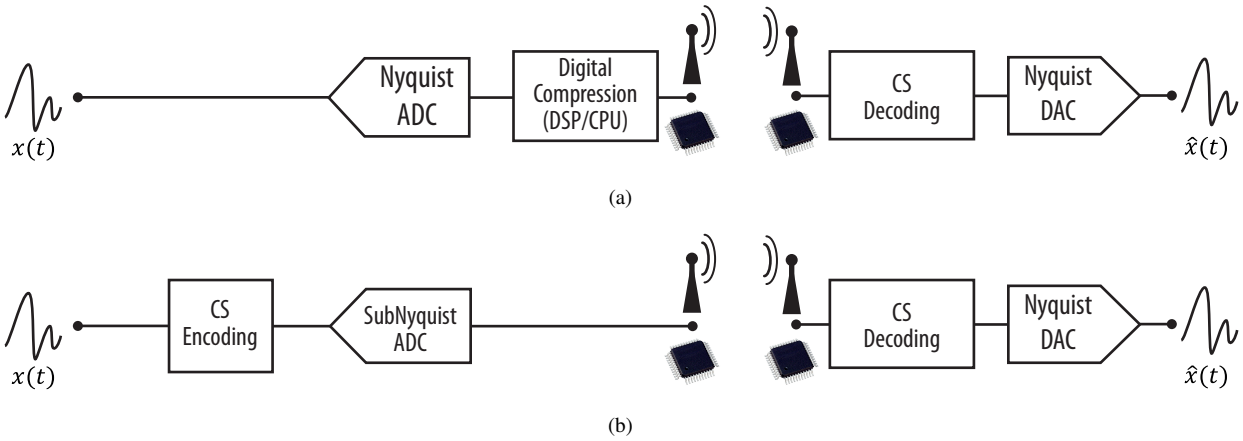


Fig. 1. Basic block diagrams for compression/decompression systems: (a) in the conventional approach the input signal is sampled and converted into digital words at Nyquist rate, then compressed by any choice of lossless or lossy algorithm. The input signal can be recovered from the compressed representation by the proper digital decompression algorithm; (b) in the CS approach the input signal is first elaborated by the (analog) CS encoder, then sampled and converted into digital words at a sub-Nyquist rate. The CS decoder ensures the input signal reconstruction from these values.

higher than the expected level. Also in presence of a *stronger* saturation we are still capable to correctly reconstruct the signal with a minimal performance loss.

The rest of the paper is organized as follows. In Section II we recall the basic concepts and notation for a CS system, while in Section III we detail the architecture of the proposed circuit, with emphasis on non-standard adopted solutions. Then, in Section IV we present many results from measurements of the circuit, either using artificially created sparse test signals, and some real biomedical signals. Measurements on the latter ones shows the capability to get compression factors as high as 8–10. Finally, we draw the conclusion.

II. Foreword on Compressing Sensing

The entire CS theory is developed on signals $x(t)$ defined only for $0 \leq t < T_W$. This is not a limitation, since it is always possible to slice any signal of interest into pieces defined over adjacent time windows of length T_W, process them separately and then get the output signal by joining all processed slices.

The main assumption in the CS approach is to deal with a *sparse* signal. From a mathematical point of view, given an orthonormal basis $[\psi_1(t), \psi_2(t), \ldots, \psi_N(t)]$, $0 \leq t < T_W$, any possible instance $x(t)$ of a sparse signal can be written as

$$x(t) = \sum_{i=1}^{N} \psi_i(t)\, \alpha_i$$

where the *sparse representation* vector $\alpha = \{\alpha_1, \ldots, \alpha_N\}$ has only a few non-vanishing terms. In a K-sparse signal, there are at most only $K \ll N$ significant coefficients.

The CS approach aims at *sensing* $x(t)$ in a *compressive* way, i.e., by using only M measurements instead of N as in the classical theory, with $K < M < N$. The measurement vector $Y = \{y_1, \ldots, y_M\}$ is achieved by means of projecting $x(t)$ over a set of sensing function $\phi_j(t)$, $j = 1, \ldots, M$, i.e., $y_j = \langle \phi_j(t), x(t) \rangle_{T_W}$, where $\langle \cdot, \cdot \rangle_{T_W}$ stands for inner product on the time window T_W that is defined as $\langle \phi_j(t), x(t) \rangle_{T_W} = \int_{T_W} \phi_j(t) x(t) dt$.

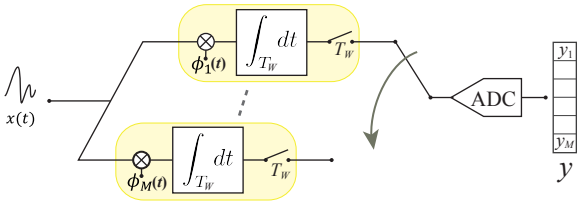


Fig. 2. Basic block diagram of the RMPI architecture with a shared ADC.

The most common and general CS architecture is the RMPI approach [15], that is schematized in Fig. 2. Here, $x(t)$ is independently processed by M channels to compute at the same time the M inner product. In the j-th channel, $x(t)$ is first multiplied with the j-th sensing function, and then integrated over a time window T_W. Measurements can be converted into digital words by a shared sub-Nyquist ADC, whose rate is M/T_W conversion per time unit, that is much smaller with respect to Nyquist rate N/T_W.

Without loss of generality in this paper we limit ourselves to the discrete-time case, where any realization of the input signal is represented by a vector $x = \{x_1, x_2, \ldots, x_N\} \in \mathbb{R}^N$, where $x_i = x(iT)$. In this case, the orthonormal sparsity basis can be written as a matrix $\Psi \in \mathbb{R}^{N \times N}$, whose columns are the basis vectors, such that

$$x = \Psi \alpha$$

The M measurements are still obtained by means of the inner product between x and a set of M sensing vectors $\phi_j \in \mathbb{R}^N$

$$y_j = \langle \phi_j, x \rangle_N = \sum_{i=1}^{N} \phi_{j,i} x_i \tag{1}$$

where with $\phi_{j,i}$ we indicate the i-th element of the j-th sampling vector. By defining the sampling matrix $\Phi \in \mathbb{R}^{M \times N}$ whose M rows are the sensing vectors, Y is given by

$$Y = \Phi x = \Phi \Psi \alpha = A \alpha \tag{2}$$

where $A \in \mathbb{R}^{M\times N}$ is a matrix that directly links the measurement vector with the sparse representation. Note that in any actual system, (2) may be rewritten as

$$\hat{Y} = \Phi x + \nu = A\alpha + \nu \tag{3}$$

where ν represents and additive vector that takes into account both analog noise and system non-idealities, as well as the quantization noise.

The CS decoder estimates α (and so x) from Y (or $\hat{Y}$ for noisy systems) under the assumption that Ψ and Φ (and so A) are known. This is an algebraic problem, since one should simply invert (2) to get α from Y. However A is rectangular with $M<N$, so the problem is ill-posed. Roughly speaking, there is an infinite number of realization α such that $A\alpha = Y$. To overcame the impasse, one should look at the sparsest solution $\hat{\alpha}$ given by the minimization problem

$$\begin{aligned} \hat{\alpha} &= \arg\min_{\alpha} \|\alpha\|_1 \\ \text{s.t.} &\left\| A\hat{\alpha} - \hat{Y} \right\|_2 < \varepsilon \end{aligned} \tag{4}$$

where $\|\cdot\|_1$ and $\|\cdot\|_2$ stand respectively for the l_1 and l_2 norms, and ε covers the effects of ν. The input signal is reconstructed as $\hat{x} = \Psi\hat{\alpha}$.

The CS theory ensures correct reconstruction if Φ verifies the *restricted isometry property* (RIP) [16], i.e., A is able to preserve the norm of α. The intrinsic lower bound on the required number of measurement M is made by

$$M \geq CK \log\left(\frac{N}{K}\right) \tag{5}$$

where C is a constant typically set around 4 [2]. To verify RIP, Φ can be conveniently implemented as a *binary antipodal* matrix, i.e., $\phi_{j,i} \in \{-1, 1\}$, relaxing the product operations required to compute the inner products into much simpler sign inversion operations, an thus allowing a simpler hardware implementation at no costs in terms of CS performance reduction [4].

Many algorithms have been proposed to solve problem (4) under the assumption (5). In the following we use that known as SPGL1 [17], that belong to the class of iterative CS solvers. Furthermore, we also follow the approach known as *rakeness* [18], that allows to increase CS performance either increasing reconstruction signal quality at M constant, or decreasing M at a constant reconstruction signal quality. The goal of the rakeness approach is to increase the energy collected in the sensing stage by a statistical matching between x and ϕ_j, and at the same time preserving the RIP of the A matrix.

Mathematically, and referring to the discrete time case, let us model ϕ_j and x as realizations of two stochastic processes $\underline{\phi}$ and $\underline{x}$. We define the *rakeness* ρ as

$$\rho(\underline{\phi}, \underline{x}) = \mathbf{E}_{\underline{\phi},\underline{x}}\left[\left| \langle \phi_j, x \rangle_N \right|^2 \right]$$

where $\mathbf{E}_{\underline{\phi},\underline{x}}$ stands for the expected value with respect to both processes $\underline{\phi}$ and $\underline{x}$. The idea is to increase the energy collected by the generic ϕ_j with the constraint that the sensing vectors are random enough to preserve the RIP. This translates into the following optimization problem:

$$\begin{aligned} \max_{\underline{\phi}} \quad & \rho(\underline{\phi}, \underline{x}) \\ \text{s.t.} \quad & \langle \phi_j, \phi_j \rangle_N = e \\ & \rho(\underline{\phi}, \underline{\phi}) \leq \tau e^2 \end{aligned} \tag{6}$$

where e is the energy of each sampling vector[1] while τe^2 is an upper bound of the $\underline{\phi}$ correlation. The tuning τ is not critical, since it does not appreciably alter the overall system performance [19].

This approach will be considered in the examples of Sec. IV-D to greatly reduce the number of measurements necessary for the acquisition of real biomedical signals.

III. AIC Prototype Architecture

Starting from the block diagram of Fig. 2, we have designed a 16-channel RMPI-based AIC prototype. The core of the proposed circuit is a low-power fully-differential switched-capacitor (SC) integrator that implement a binary antipodal modulation, where multiplication with the $\phi_{i,j}$ is simply achieved by means of switches that swap the differential input signal pair.

In the following we describe the circuit behavior with emphasis on non-classical solutions to cope with some hardware-related CS issues, in particular:

- time continuity ensured for processing all signal slices;
- saturation of the SC integrator;
- data corruption by leakage currents.

We will address all of them, respectively, in Sec. III-A, III-B and III-C. Performance of RMPI channels are summarized in Table I.

The prototype also embeds a low-power Successive Approximation Register (SAR) based ADC. It is based on a fully differential architecture, with two differential capacitive array dividers, and can operate at a rate up to $200\,\mathrm{kS/s}$. The architecture of the SAR is detailed in Section III-D.

A. Switched Capacitor RMPI with time continuity

The architecture of a single RMPI channel (including the output buffer that is shared between all 16 channels) is detailed in Fig. 3. Basically, it can be described as a standard fully-differential SC integrator, with differential input signal $x^D(t) = x^+(t) - x^-(t)$ and common mode voltage V_{CM}, and regulated by the two non-overlapping clock signals PHI_1 and PHI_2 of period T. The main differences with respect to a standard SC integrator can be summarized in two additional switches at the input stage to select whether the signal to be integrated is $x^D(t)$ or $-x^D(t)$, and two couples of feedback capacitors C_F^I and C_F^{II} with same value $C_F^I = C_F^{II} = C_F$.

The latter capacitors are used to solve the problem of ensuring continuity between successive slices of the input signal. Referring to Fig. 2, this issue can be described as follows. Let us assume that all M RMPI channels are processing the same slice. At the end of the time window, the M integrations

[1]Note that for antipodal sampling sequences it is always $e = N$.

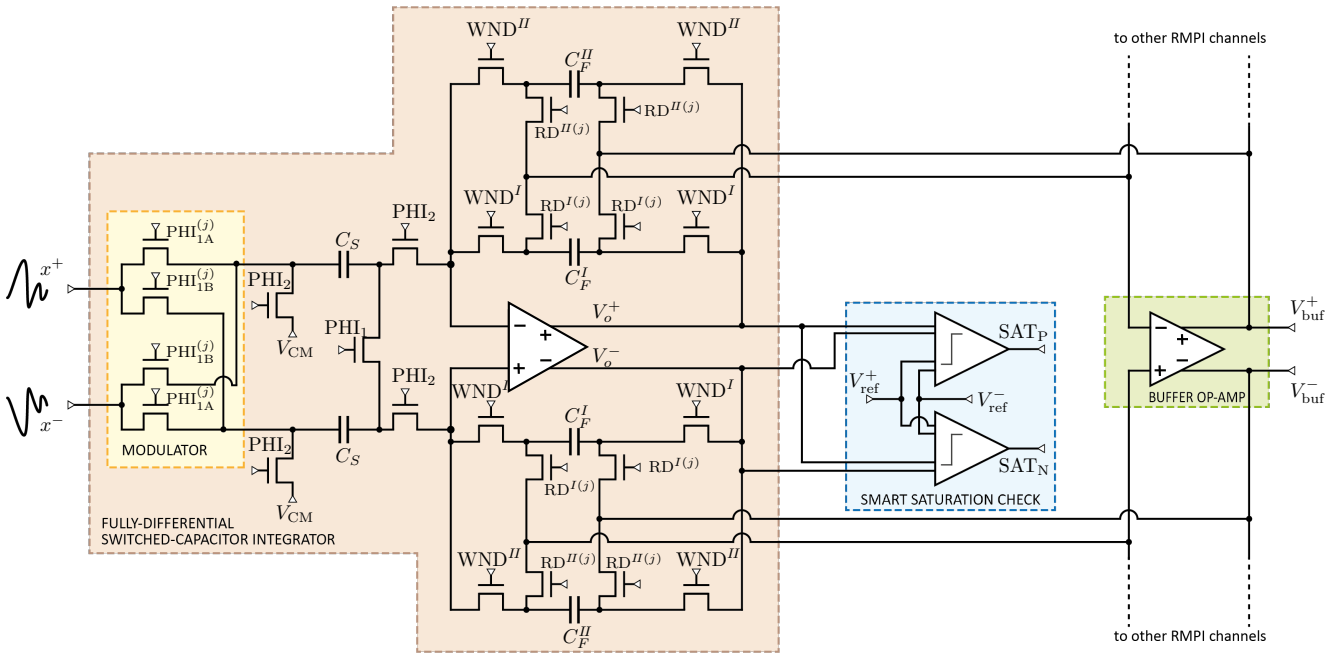


Fig. 3. Detailed architecture of the switched capacitor circuits implementing a single RMPI channel in the designed prototype, including the buffer shared between all RMPI channels.

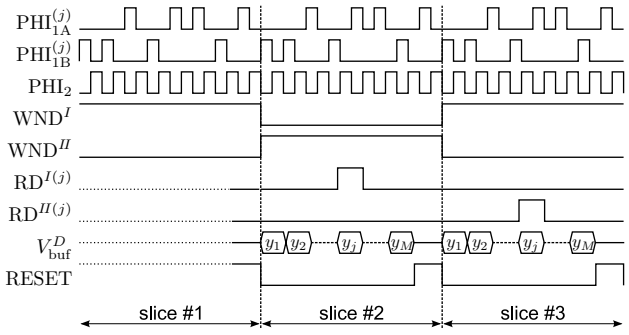


Fig. 4. Timing diagram for signals controlling the behavior of the j-th RMPI channel.

are complete and measurements are available. However, before processing a new slice of signal, the accumulated values have to converted by the DAC and, after that, integrators must be resetted, i.e., the charge accumulated on the feedback capacitor has to be cleared. Either these two operations (i.e., conversion and charge clearance) have to be performed in a negligible time, or the same hardware cannot be used to process the successive slice of the input signal. Connecting alternatively the two couples of capacitors C_F^I and C_F^{II} to the op-amp solves this problem.

In details, the circuit behavior is the following. Let us consider the j-th RMPI channel computing $y_j = \langle \phi_j(t), x(t) \rangle_{T_W}$, and let us refer to the control signals timing diagram depicted in Fig. 4. In odd time windows, the signal WND^I is high while WND^{II} is low, so the feedback capacitors C_F^I are connected to the op-amp, while the C_F^{II} are disconnected. In the i-th sampling phase the control signal PHI_1 is asserted along with either $\mathrm{PHI}_{1\mathrm{A}}^{(j)}$ (when $\phi_{j,i} = 1$) or $\mathrm{PHI}_{1\mathrm{B}}^{(j)}$ (when $\phi_{j,i} = -1$), thus connecting either $x^D(t)$ or $-x^D(t)$ to the C_S. At the end of the sampling phase the charge stored on C_S, assuming a 50% duty cycle, is $Q_S = C_S\, \phi_{i,j}\, x^D(iT - T/2)$.

Then, in the evaluation phase PHI_1, $\mathrm{PHI}_{1\mathrm{A}}^{(j)}$ and $\mathrm{PHI}_{1\mathrm{B}}^{(j)}$ are reset and PHI_2 is asserted, and Q_S is moved to the C_F^I. At the end of this transient, the differential op-amp output voltage $V_o^D = V_o^+ - V_o^-$ is

$$\begin{aligned} V_o^D(iT) &= -\frac{C_S}{C_F} \sum_{z=1}^{i} \phi_{z,j}\, x^D\left(zT - \frac{T}{2}\right) \\ &= g \sum_{z=1}^{i} \phi_{z,j}\, x^D\left(zT - \frac{T}{2}\right) \end{aligned}$$

where $g = -C_S/C_F$ is the gain of the integrator.

After the N-th step, i.e. after a time $NT = T_W$ the integration is completed and the output op-amp differential voltage is the desired measurement

$$y_j = V_o^D(T_W) = g \sum_{i=1}^{N} \phi_{i,j}\, x^D\left(iT - \frac{T}{2}\right) \tag{7}$$

The only remarkable difference between (1) and (7) is the integrator gain g.

At the same time instant when this time window ends and the successive one begins, WND^I goes low and WND^{II} high. The capacitors C_F^I are therefore disconnected from the op-amp and they keep sampling the y_j value, while C_F^{II} (assumed uncharged) are connected and a new integration can starts immediately. Then, the C_F^I from all stages are sequentially connected to the buffer op-amp (signal $\mathrm{RD}^{I(j)}$ asserted), thus either charging the internal ADC input buffer or making the measurements externally available as a differential voltage signal. After that, a RESET signal (not shown in Fig. 3 for the sake of simplicity) is provided, and the C_F^I are completely

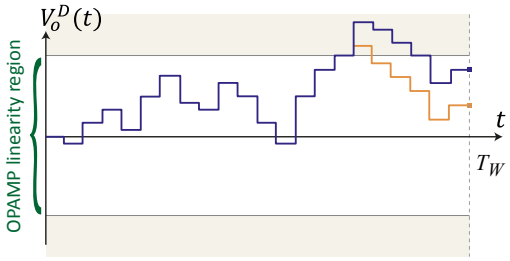


Fig. 5. Saturation of the op-amp may result in an actual $V_o^D(t)$ (dark line) completely different from the ideal expected one (ligth line), ending in a *corrupted* measurements.

discharged, making them ready to be used in a new integration process.

The advantage of this approach is to ensures time continuity at a small cost in terms of area requirements, but at no cost in terms of power. In fact, we need only a replication of the C_F and a few additional small switches, but no active devices such as amplifiers or active sample/hold circuits.

B. Saturation Checking

The two comparators that can be seen in Fig. 3 are embedded in all RMPI channels, and are used to check if the intermediate accumulated voltage $V_o^D(iT)$ goes above or below the two threshold levels V_{ref}^D and $-V_{\text{ref}}^D$ (with $V_{\text{ref}}^D = V_{\text{ref}}^+ - V_{\text{ref}}^-$), as suggested in [14]. In case, a flag signal (either SAT_P or SAT_N) is generated, and the time instant i is recorded and passed to the reconstruction algorithm instead of the y_j.

The advantage of this approach is twofold and it is very well explained in [14]. As a brief summary, we can say that from the one hand we can detect and avoid *corrupted* measurements. The main problem here is not that the measurement $y_j = V_o^D(T_W)$ may fall outside of the conversion range of the ADC [20]. This event in fact can be easily detected, as these measurements are automatically converted either to the maximum or minimum digital value, and can be ignored by the reconstruction algorithm. If instead the $V_o^D(iT)$ reaches the op-amp saturation level at a time step i smaller than N, then the final value $V_o^D(T_W)$ is irreparably corrupted, as in the example of Fig. 5. Note that, depending on the values of Φ_j and x for time steps between i and N, the $V_o^D(T_W)$ may fall in the ADC conversion range. Looking at the $V_o^D(T_W)$ is not useful for the detection of these events.

On the other hand, we can remember that the philosophy underlying the entire CS framework is to recover a signal with the lowest possible amount of information. Under this point of view, discarding saturated measurements may lead to a quantity of information insufficient to correctly reconstruct the signal. On the contrary, the time instant i when the saturation event is detected contains almost the same information as the uncorrupted y_j value, and may be used instead of the y_j by the reconstruction algorithm for signal reconstruction as explained in [14].

Note that the overhead in terms of area and power consumption for applying this strategy is very limited, since only two comparators are required, that can be designed as dynamic and without any particular speed or accuracy requirement. With this approach, as shown in the example of Sec. IV-B it is possible to achieve correct signal reconstruction even in presence of more than 60% of measurements saturated.

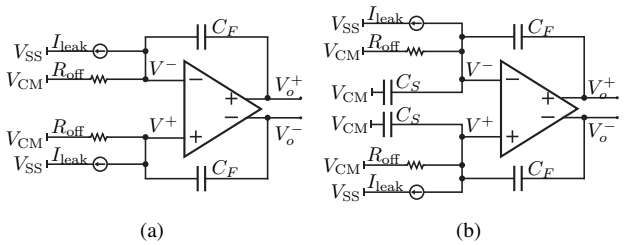


Fig. 6. Simplified equivalent SC circuit model for computing the effects of leakage currents. (a): Sampling phase; (b): evaluation phase.

C. Leackage effects

Almost all biomedical signals exhibit their sparsity properties when the integration time T_W is long, sometimes up to a few seconds [9], [21]. Using an AIC not specifically designed to work with very long T_W may result in poor performance.

Referring to the proposed architecture, if T_W is too long then the charge accumulated into either the C_F^I or the C_F^{II} may be corrupted by leakage currents. This issue must be taken into account in the design of the circuit.

Without entering into details, we can use the simplified equivalent circuit of Fig. 6(a) for sampling phase, and of Fig. 6(b) for the evaluation phase, to model the leakage on each RMPI channel. The R_{off} and the I_{leak} are used to model, respectively, the source/drain current of all MOS switches in the off state, and the source/bulk and drain/bulk junctions inverse current, and have been computed according to used CMOS technology.

The evolution of the two circuits is very easy to study, resulting in negative exponential voltage drops. In more detail, there is a common mode drop at the op-amp inputs, and a differential drop at the op-amp outputs. In both phases, the input common mode drop is fast, with a final voltage level equal to $V_{CM} - R_{\text{off}} I_{\text{leak}}$. If the input common mode range of the op-amp is large enough, then this voltage drop is not an issue.

On the contrary, the differential output drop is very slow (the associated time constant is in both cases $\approx A_d C_F R_{\text{off}}$) but the drop is also linearly increasing with V_{off}. To keep this effect as low as possible, we need a high A_d and a low V_{off}, with a R_{off} as high as possible.

In the design of the circuit we limited the effect of R_{off} and I_{leak} by using very small NMOS switches. By using a proper op-amp design, and increasing the feedback capacitors to $C_F = 40\,\text{pF}$, we expect a differential voltage drop comparable to the ADC less significant bit (LSB) for a $T_W \approx 1\,\text{s}$, that is enough for all biomedical signals of interest.

D. SAR ADC

The designed ADC is a standard 11-bit fully differential converter based on a Successive Approximation Register

RMPI performance	
capacitors value	$C_S = 5\,\text{pF}$, $C_F = 40\,\text{pF}$
gain	$g = -1/8$
area	$850 \times 280\,\mu\text{m}^2$
step-response settling time	$3\,\mu\text{s}$
data retention	$\approx 1\,\text{s}$
Op-amp performance	
architecture	class-A telescopic cascode
power consumption	$27\,\mu\text{W}$ ($15\,\mu\text{A}$@$1.8\,\text{V}$)
A_d	98 dB
GBW	480 MHz
V_{off}	$< 0.4\,\text{mV}$ (1)
CMR	$[0.39\,\text{V}, 1.58\,\text{V}]$

(1) Estimated from MonteCarlo simulations.

TABLE I
DESIGN PERFORMANCE SUMMARY FOR THE SWITCHED CAPACITOR RMPI INTEGRATOR.

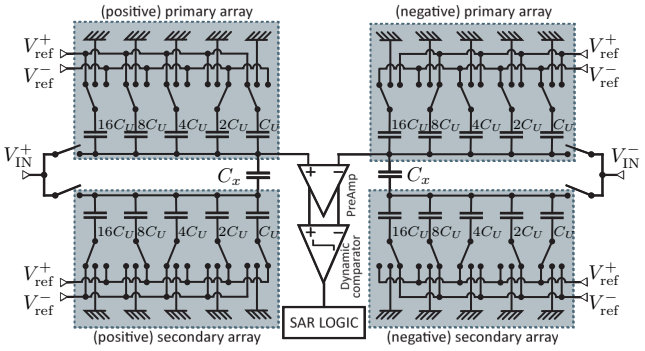


Fig. 7. Basic architecture of the SAR ADC.

(SAR) architecture [22]. The schematic is depicted in Fig. 7, and it is based on two couples of split capacitor arrays (a main couple and a secondary couple) with unit capacitance $C_U = 470\,\text{fF}$, that scale the sampled voltage by means of charge redistribution to obtain successive approximations of the conversion. Due to the differential architecture, the first bit is obtained by a direct comparison between the differential pair generating the input signal, while other 5 bits are achieved by switching the main array, and 5 additional bits by switching the secondary one. Main and secondary arrays are connected together by a capacitance $C_x = C_U$ as in [23]. The comparator is based on a dynamic clocked architecture, and it is driven by a very small and low-power static preamplifier to decouple the comparator from the two arrays, thus increasing performance.

IV. Circuit Measurements

The circuit described in Sec. III has been designed and fabricated in Texas Instruments $180\,\text{nm}$ $1.8\,\text{V}$ CMOS technology. The microphotograph of the circuit is depicted in Fig. 8. The total chip size is $2.3 \times 3.7\,\text{mm}^2$ ($2.6 \times 4.0\,\text{mm}^2$ including pads).

The designed integrated circuit embeds 16 RMPI channels and the 11 bit SAR ADC. The digital control logic (excluding that of the SAR) has not been embedded for maximum versatility, and all the measurements presented here have been obtained controlling the designed circuit with a Xilinx Spartan 3E FPGA. The FPGA also controls an external digital-to-analog converter that is used to generate the reference voltages and the differential input test signal.

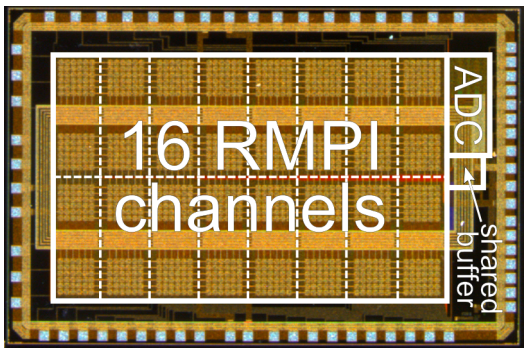


Fig. 8. Microphotograph of the designed integrated circuit.

Parameter	Value
Area	$320 \times 770\,\mu\text{m}^2$
power consumption ($100\,\text{kS/s}$)	$10.08\,\mu\text{W}$
Dynamic Range ($100\,\text{kS/s}$, $f_{\text{in}} = 100\,\text{Hz}$)	64.2 dB
enob	8.99 bit
INL	$< 3.4\,\text{LSB}$
max. conversion speed	$200\,\text{kS/s}$
Figure of Merit ($100\,\text{kS/s}$)	198 fJ/c.-l.

TABLE II
SAR-BASED ADC PERFORMANCE SUMMARY.

In the following we present four different sets of measurements. The first one (Sec. IV-A) is used to measure performance of the SAR converter. In Sec. IV-B we show measurement on the overall compressed sensing system using artificially created signals, while in Sec. IV-C the same signals are used with increasing amplitude to test the system in presence of saturation events. Finally, we create (Sec. IV-D) a realistic setting by implementing an electrocardiogram (ECG) and electromyogram (EMG) coming from the PhysioNet database [24] as test signals.

A. SAR ADC

The performance of the ADC is summarized in Table II. The integral non-linearity (INL) is within $3.4\,\text{LSB}$ at 11 bit resolution – see Fig. 9(a) –, the spurious free dynamic range is measured as $64.2\,\text{dB}$ – see Fig. 9(b) – and the effective number of bits (enob) is evaluated in approximately 9 bit. With a measured power consumption of $6.3\,\mu\text{W}$ at $100\,\text{kS/s}$, the figure of merit of the ADC is $198\,\text{fJ/conversion-level}$.

B. AIC, synthetic sparse signal tests

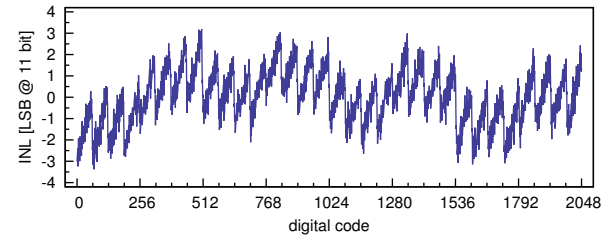
To properly test all the features of proposed AIC, we have designed two ad-hoc different setups based on two artificially created sparse signals.

In the first setup, we have generated an input signal sparse on the canonical base, i.e. on the unit pulse base:

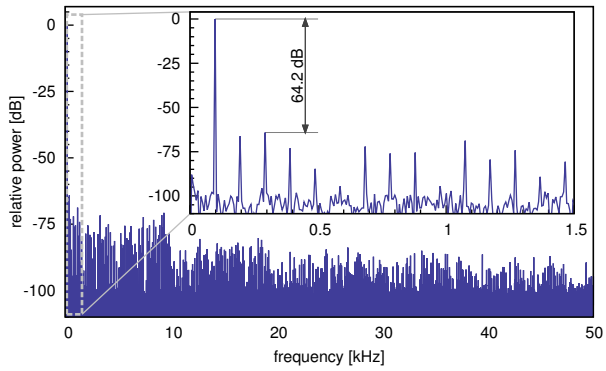
$$x(t) = \sum_{i=1}^{N} \alpha_i \, \text{u}\,(x/T - i) \tag{8}$$

where $\text{u}(t) = 1,\ 0 < t < 1$ and 0 elsewhere is the normalized unit pulse.

We set $N = 20$ and a sparsity level $K = 2$, i.e. only 10% of the α_i are different from zero. According to (5),



(a)



(b)

Fig. 9. Performance of the the SAR-based ADC. (a): Integral non-linearity; (b): spurious free dynamic range.

the minimum number of measurements required for a correct signal reconstruction in this setting is $M = 8$. Accordingly, we enable only the first 8 RMPI channels of the designed circuit.

As an example, given the input signal sparse representation

$$\begin{aligned} \alpha_2 &= 1.44\,\mathrm{V} \\ \alpha_7 &= 0.36\,\mathrm{V} \\ \alpha_i &= 0, \quad i \neq 2, i \neq 7 \end{aligned} \tag{9}$$

then the j-th measurement depends only on $\Phi_{j,2}$ and $\Phi_{j,7}$, and more precisely, accordingly to (7)

$$y_j = \begin{cases} -225\,\mathrm{mV} & \Phi_{j,2} = 1 \text{ and } \Phi_{j,7} = 1 \\ -135\,\mathrm{mV} & \Phi_{j,2} = 1 \text{ and } \Phi_{j,7} = -1 \\ 135\,\mathrm{mV} & \Phi_{j,2} = -1 \text{ and } \Phi_{j,7} = 1 \\ 225\,\mathrm{mV} & \Phi_{j,2} = -1 \text{ and } \Phi_{j,7} = -1 \end{cases} \tag{10}$$

The differential output V^D_{buf} of the internal buffer (see Fig. 3) for this example has been made externally available, and is shown in Fig 10. In the figure we can clearly identify the 8 measurements serially outputted by the multiplexer, as well as the 4 possible cases computed in (10).

For this class of signal, an ideal RMPI system with an 11 bit quantization would theoretically achieve a reconstruction SNR of 53.2 dB. By using the designed prototype with $T = 360\,\mu$s i.e. a SC frequency equal to $f_s = 1/T = 2.78\,$kHz, we get an average measurements SNR (i.e., an SNR of the actual y_j with respect to the ideally expected ones) equal to 39.6 dB, and an average reconstruction SNR equal to 37.7 dB. An example showing both the input signal and the reconstructed signal over 5 consecutive time windows is depicted in Fig. 11.

For a more complex setup we have considered a synthetic

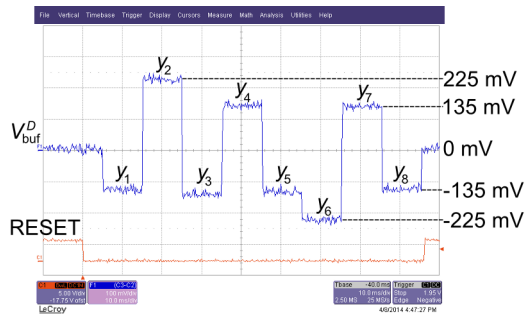


Fig. 10. Differential internal buffer output voltage (top trace) of the for the example of Sec. IV-B, showing the 8 measurements serially outputted by the multiplexer, and distributed according the 4 possible cases computed in (10). The bottom trace is the RESET signal.

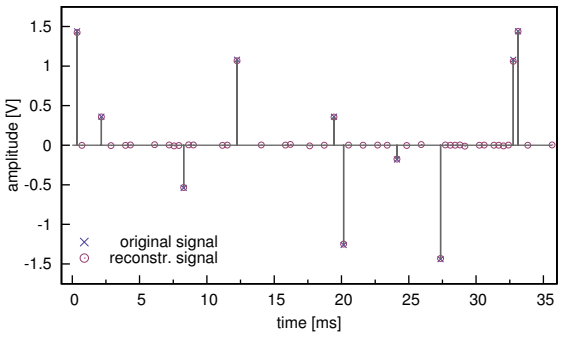


Fig. 11. Example of reconstruction of a signal with $N = 20$, $K = 2$ and $M = 8$ sparse on the canonical base, 5 time windows with $T_W = 7.2\,$ms are plotted. Steps with non-vanishing amplitude are highlighted with a marker.

signal sparse in the Fourier basis, i.e.,

$$x(t) = \sum_{i=1}^{N/2-1} \alpha_i \sin(i\,t) + \sum_{i=N/2}^{N} \alpha_i \cos((N-i)t) \tag{11}$$

For this setup, we have set $N = 64$ and $K = 3$. Under this setting, to ensure correct reconstruction we get from (5) that $M \geq 16$, i.e., we used all RMPI channels. With this setting, an ideal system would achieve a reconstruction SNR of 53.4 dB. In the designed prototype, with $T = 360\,\mu$s, i.e. $f_s = 2.78\,$kHz, measurements indicate an average SNR of 40.9 dB for the y_j, and a reconstruction SNR of 30.0 dB. The

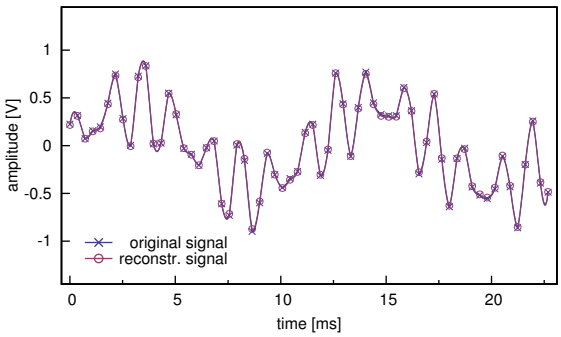


Fig. 12. Example of reconstruction of a signal with $N = 64$, $K = 3$ and $M = 16$ sparse on the Fourier base, a single time windows with $T_W = 23\,$ms is plotted. Actual sampling points are highlighted with a marker.

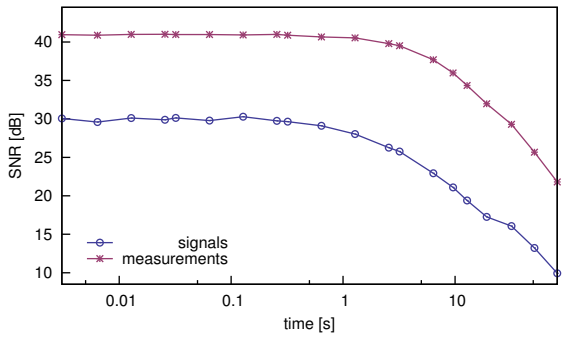


Fig. 13. Measurement SNR and reconstruction SNR for the Fourier sparse signal with $N = 64$, $K = 3$ and $M = 16$, for different time window lengths T_W.

	canonical basis	Fourier basis
setting	$N = 20$, $K = 2$	$N = 64$, $K = 3$
frequency	$f_s = 2.78\,\text{kHz}$	$f_s = 2.78\,\text{kHz}$
time window length	$T_W = 7.2\,\text{ms}$	$T_W = 23\,\text{ms}$
measurements	$M = 8$	$M = 16$
theoretical rec. SNR	$< 53.2\,\text{dB}$	$< 54.4\,\text{dB}$
power consumption	$251\,\mu\text{W}$	$495\,\mu\text{W}$
measurement SNR	$39.6\,\text{dB}$	$40.9\,\text{dB}$
reconstruction SNR	$37.7\,\text{dB}$	$30.0\,\text{dB}$
max. working frequency	–	$f_s < 125\,\text{kHz}$
max. time windows length	–	$T_W < 1.6\,\text{s}$

TABLE III
PERFORMANCE SUMMARY FOR TESTS BASED ON SYNTHETIC SIGNALS.

input and the reconstructed signal for this example in a single time window have been depicted in Fig. 12.

The latter setting has been also used for testing the behavior of the circuit at different clock speed. In particular, the maximum working speed for the designed circuit has been measured in approximately $f_s = 125\,\text{kHz}$. For any clock speed below this limit, the measurements SNR is approximately constant around $41\,\text{dB}$, and the reconstruction SNR is about $30\,\text{dB}$.

The lower bound in speed is given by the leakage currents as described in Sec. III-C. Performance for different f_s is shown in Fig. 13. In the figure we have plotted both measurements SNR and reconstruction SNR as functions of the integration window length $T_W = N/f_s$, that is the actual parameter determining the voltage drop due to leakage. We can see that performance is constant up to T_W in the order of magnitude of the second. If we define the maximum integration time as the T_W where we have a $3\,\text{dB}$ reconstruction SNR loss, we have $T_W < 1.6\,\text{s}$. This validates the developed leakage model, and ensures that the designed chip can be correctly employed for the acquisition of biomedical signals.

A performance summary of all examples considered in this section can be found in Table III.

C. Saturation checking Test

In this section we present results achieved when scaling the Fourier-based signal of Sec. IV-B and depicted in Fig. 12 by a factor $0 < s \leq 2$. For $s \leq 1$ none of the RMPI channels reaches final or intermediate saturation; furthermore for $s = 1$ the signal is the same as in the aforementioned settings,

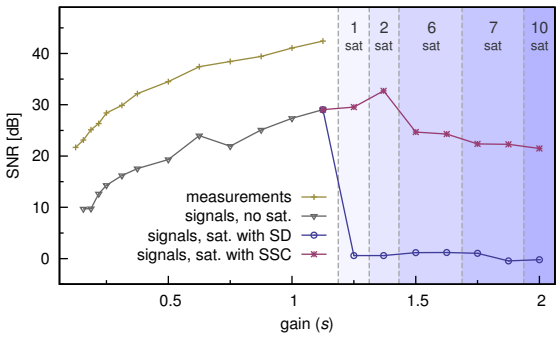


Fig. 14. Performance of the Fourier-based example at different signal gain s. The plot include both measurements SNR and reconstruction SNR when adopting the proposed smart saturation check (SSC) and when saturated measurements are simply dropped (SD). The number of saturated measurements per time window is also indicated.

and measurements y_j exploit all the ADC conversion range. However, for values larger than $s = 1$, some saturation events are observed. Results can be observed in Fig. 14.

For very low values of s we can observe a low performance, since the quantization noise introduced by the ADC is relevant with respect to the power of the input signal and so of the y_j. As s increases, also the power of the y_j increases, and we observe a better measurements SNR and a better reconstruction SNR.

For $s > 1$ we cannot define anymore a measurement SNR, and we need to use the instants of saturation events to recover the input signal as in Sec. III-B. Intriguingly, performance is still increasing with s when only a limited number of saturation events are detected. This can be intuitively explained as due to two effects. On the one hand, in this region the quantity of information achieved from saturation instants almost matches that of the y_j. On the other hand, the values of non-saturated measurements is increasing with s, and so their conversions accuracy.

When the number of saturated measurements further increases, both the quantity of available information on the signal and the system performance decrease. However, we are still able to reconstruct the input signal with an acceptable SNR. Note that for $s = 2$ we still have approximately $22\,\text{dB}$ of reconstruction SNR with 10 out of 16 measurements that reach saturation.

To fully understand the advantages of the saturation checking approach, we can compare results achieved when reconstruction is performed only with *good* measurements, i.e., when dropping measurements when a saturation event is detected as suggested in [20]. This case is also plotted in Fig. 5. Since M is taken as its minimum value according to (5), dropping saturated measurements reduces the data available to the CS decoder to an insufficient level, and we are not able anymore to correctly reconstruct the input signal. As we can see in the figure, the reconstruction SNR has an abrupt fall at $s \approx 1$.

In conclusion, when using the saturation checking approach, optimal results are achieved when s is slightly larger than 1, then it gradually decreases. This is extremely important, since allow us to work with signals with high amplitude so exploit-

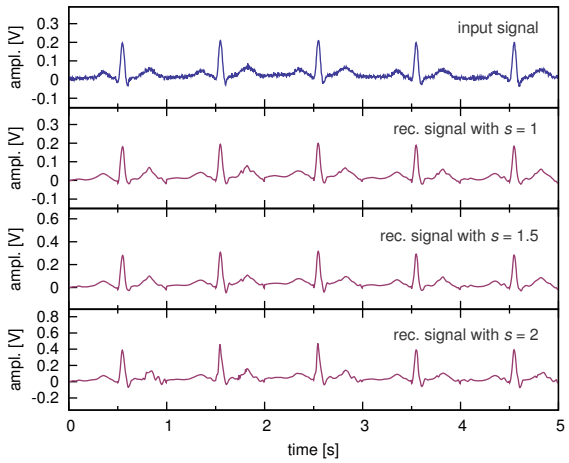


Fig. 15. Example of a real ECG signal with $f_s = 256\,\text{Hz}$, $N = 128$ (10 consecutive time windows are plotted). From top to bottom: input signal, reconsructed signal with scale factor $s = 1$, $s = 1.5$ and $s = 2$.

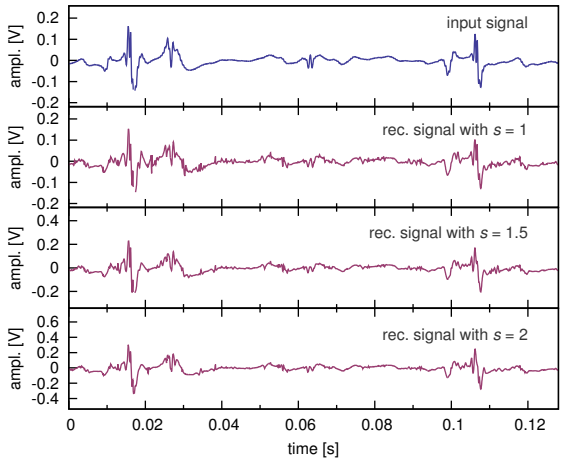


Fig. 16. Example of a real EMG signal with $f_s = 20\,\text{kHz}$, $N = 256$ (10 consecutive time windows are plotted). From top to bottom: input signal, reconsructed signal with scale factor $s = 1$, $s = 1.5$ and $s = 2$.

ing all the ADC dynamic and reducing the quantization noise effect. Note that in classical approaches this is not possible, since s has always to be kept within a "safe range" in order to avoid saturation and an abrupt decrease in performance in case the input signal has an unexpected high peak value.

D. Test with real biomedical signals

We consider here two realistic cases of biomedical signals both taken from the PhysioNet public database [24].

In the first one we generate an ECG signal with an approximately heart-beat of $1\,\text{Hz}$ from a patient with no diseases. The signal is sampled at $f_s = 256\,\text{Hz}$ and we use a time windows of length $T_W = 0.5\,\text{s}$, so $N = 128$. The sparsity basis used for signal reconstruction is the Symlet-6 family of the Wavelet functions [25]. In order to maximize performance, we generate the Φ_j sequences according to the *rakeness* approach. This allows us to correctly reconstruct the signal using only 16 measurements. Furthermore, we also considered the input signal with three different scale factors, i.e., $s = 1$ where the amplitude of the signal is the maximum one that generates no saturation events; $s = 1.5$ with an average number of 0.4 saturation events per time window, and $s = 2$, when 1.5 saturation events are detected per time windows. Results are shown in Fig. 15 and, despite the fact that a reconstruction SNR is difficult to define since the input signal has an intrinsic and undefined noise, show that in all three cases the reconstructed signals keep the same features of the original signal with a compression factor equal to $N/M = 8$.

In the second one we consider and EMG signal of an healthy patient. The EMG signal is usually sampled at a frequency of about $20\,\text{kHz}$, and then downsampled [9], [21]. Here, since the designed circuit is capable to work at high frequencies, we can consider $f_s = 15 - -20\,\text{kHz}$ and elaborate the signal without downsampling. In this setting we consider $N = 256$, with $T_W = 12.8\,\text{ms}$. The considered sparsity basis is, as in the previous example, given by the Symlet-6 Wavelet functions, and we exploit the rakeness approach. However, due to the high value of N, we have to set $M = 24$, i.e., more than one test chip has to be used.

Results are shown in Fig. 16 for three different scale factors s. Again, we can see the capability to reconstruct the input signal without losing its main features for $s = 1$ where no saturation events are detected, for $s = 1.5$ when an average number of 1.2 saturation events per time window is detected, and also for $s = 2$ with 2.5 saturation events per time windows. The compression rate in this example is equal to $N/M \approx 10$.

V. Conclusion

In this paper we have presented an AIC exploiting the CS paradigm. The converter has been designed and fabricated in Texas Instruments $180\,\text{nm}$ CMOS technology and its typical applications are given by biomedical signals. As additional feature, the prototype includes a smart and innovative signal saturation checking mechanism, that allows to reconstruct the input signal even in presence of saturation with negligible costs in terms of hardware requirements. Measurements on artificial signals and on real biomedical signals confirms the capability of the prototype to acquire a signal with compression gains up to 8–10.

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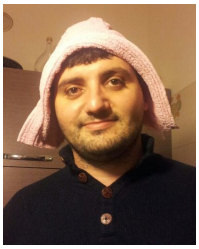
Fabio Pareschi is the chip designer and He is also an handsome guy.



Mauro Mangia is the OINK inventor, and the #1 in signal generation.