40 Volt NMOS in a 0.5 µm Standard CMOS Process

Tsung-Hsueh Lee and Pamela A. Abshire
Dept. of Elect. & Comp. Eng. and Inst. for Syst. Research
University of Maryland, College Park, MD, USA
{thlee, pabshire}@umd.edu

Abstract—**High-voltage NMOS structures were implemented by introducing a lightly doped drain area to separate the channel and the drain diffusion area for NMOS transistors, and by extending the poly layer over the intervening field oxide. Majority and minority carrier guard rings were used to minimize parasitic effects and isolate the devices. A family of high-voltage devices was implemented with various geometries in order to determine the optimal dimensions. A total of 16 square and 16 circular devices were fabricated in a 0.5 µm standard 5V CMOS technology. Measurement results demonstrate breakdown voltages as high as 40 V in comparison with 10.9 V for a standard transistor in the same run. Breakdown voltages were found to be highest for circular structures in most cases. Circular structures also showed comparable transconductance to standard transistors. Detailed characterization such as Early voltage and threshold voltage are discussed.**

I. Introduction

Over the past 60 years, CMOS feature scaling has aggressively reduced minimum transistor sizes, with many benefits including reduced cost and power and increased speed. These advances are inherently accompanied by challenges such as reduced voltage rails and breakdown voltage of the devices. This voltage limitation introduces incompatibility with many sensing and actuation applications as well as medical instruments, aircraft, and automobiles which often require high voltages. This restricts the opportunities for dense system integration and increases overall system costs when high voltages cannot be achieved in standard CMOS and require the use of specialized technologies. Therefore, high-voltage devices in a standard CMOS process are generally enabling for many kinds of integrated sensor systems.

Implementation of high-voltage MOSFETs in a standard CMOS process often includes introducing a lightly doped drain area to separate the channel and the drain diffusion area, and extending the poly layer over the intervening field oxide [1][2]. This technique is also similar to the implementation of a lateral diffusion MOSFET [3]. In a process without p-type well, it is straightforward to implement a high-voltage NMOS by violating the design rules deliberately on the layout design and utilizing the n-well implant as the buffer region. However, implementation of a high voltage PMOS in such process requires additional implants and masks to have a similar characterization to its n-type counterpart [4]. Fortunately, many control logic circuits can be completed with only one type of high-voltage transistor under acceptable performance degradation [5]. Therefore, this paper focused on the design and optimization of a high-voltage NMOS. The comparisons between three different high-voltage NMOS structures, the design considerations, and characterization results are also included in this paper.

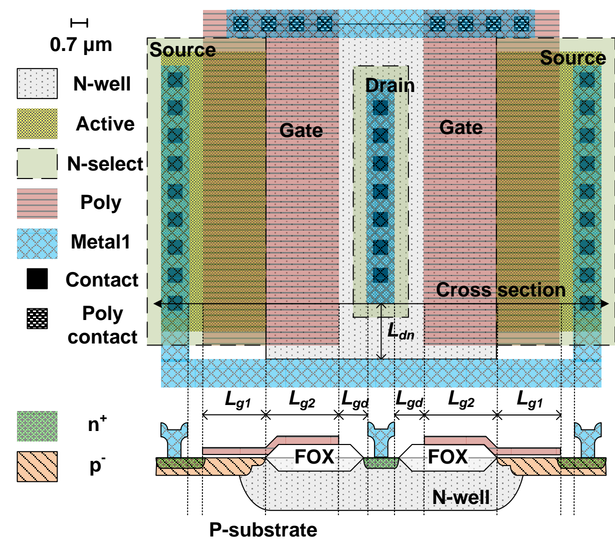

Figure 1. Layout and cross section views of the square (S) HV NMOS. p^- is from both channel-stop and threshold voltage adjust implants [2]

II. Device Design and Optimization

The implementation of a high-voltage NMOS is shown in Fig. 1 [2]. L_{g1}, L_{g2}, L_{gd}, and L_{dn} stand for channel length, field poly length, distance from poly edge to n^+ drain, and distance between of drain to n-well edge respectively. The shared drain structure can increase the area efficiency. Two techniques were used in this paper to effectively lessen two breakdown mechanisms in a MOSFET: avalanche and surface breakdown. First, the n-well region serves as a buffer region to reduce the electric field and to increase avalanche breakdown voltage at the drain side. Second, the reasons to introduce field oxide between the real drain and the channel are: 1) A highly conductive material (silicides layer) is deposited on the active region to lower the resistance of the drain and the source. The conductive material might create a direct path from the drain

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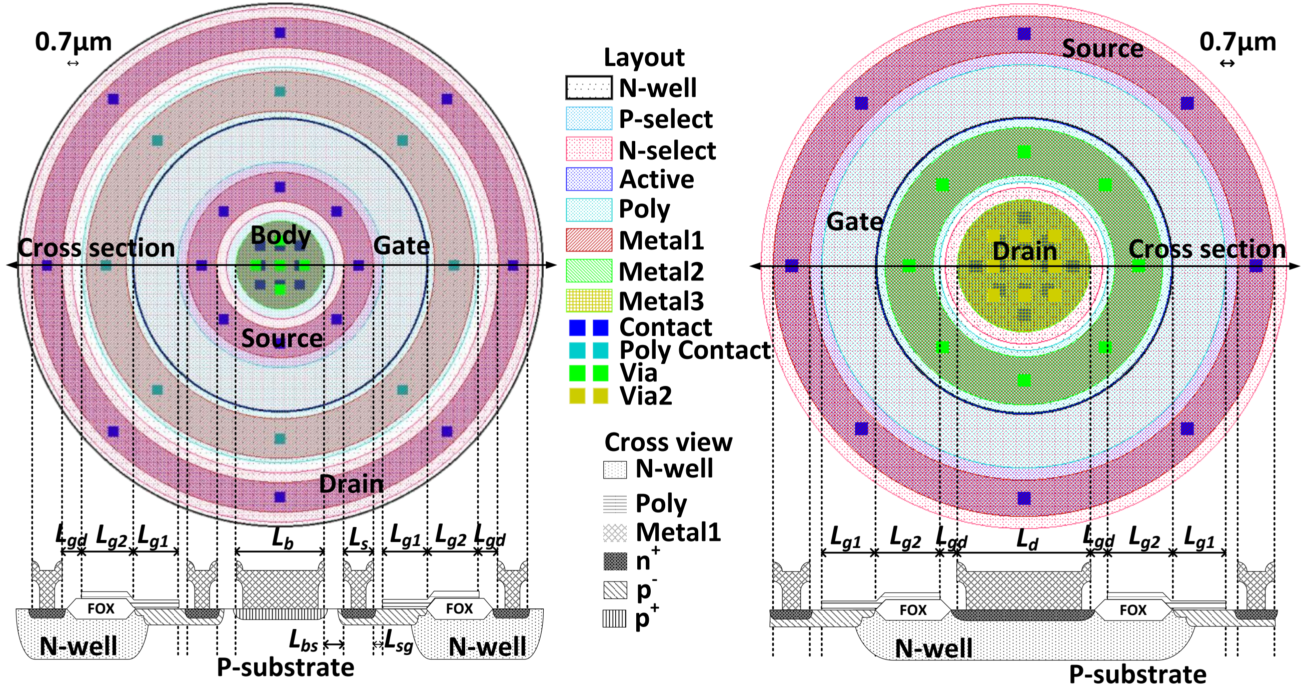

Figure 2. Layout and cross section views of two circular high-voltage NMOS structures. Circular1 (C1) is on the right; circular2 (C2) is on the left.

to the gate and cause undesired effects. The field oxide reduces the risk of such effects [6]; 2) Positive charge on the field poly will make the depletion layer at the surface of n-well expand due to charge compensation. This results in less crowded electric field lines at the surface and increases surface breakdown voltage [2].

The square layout as in Fig. 1 might cause edge breakdown and make the device hard to optimize [6][7]. Therefore, we also tried two different circular structures to reduce edge effect as in Fig. 2. L_d, L_b, L_{bs}, L_s, and L_{sg} are diameter of the center drain, diameter of the center body contacts, distance from body contacts to source, source size, and distance from source to gate. Structure circular1 is drain-centered while circular2 has body contacts surrounded by the source in the center. For these three structures majority and minority carrier guard rings (not shown in the figures) that surround the core area of the devices were used to reduce the parasitic effects and isolate the high-voltage devices from normal devices. The resulting sizes of the square devices are around 37 µm x 34 µm.

For a high-voltage device breakdown voltage is an important consideration but current-driving capability is sometimes as important. We tried different combinations of L_{g2} and L_{gd} in order to optimize these high-voltage devices and to achieve a practical balance between these two parameters. This results in 16 different combinations for the square device; for the circular device the combinations are split between the two configurations and are summarized in Table I. Other parameters were chosen as follows. L_{g1} was set to be 3.15 µm to meet the minimum channel length requirement. L_{dn} was chosen to be 2.8 µm which is given by the punch-through condition and design rules [2]. L_d, L_b, L_{bs}, L_s, and L_{sg} were chosen to be 7.7 µm, 6.3 µm, 1.4 µm, 2.1 µm, and 0.7 µm respectively. The channel width for the square device was designed to be 49 µm while that for the circular device is defined by other parameters as

$$W_{C1} = \pi \cdot (L_d + 2L_{gd} + 2L_{g2} + L_{g1}) \quad (1)$$

$$W_{C2} = \pi \cdot (L_b + 2L_{bs} + 2L_s + 2L_{sg} + L_{g1}) \quad (2)$$

where W_{C1} and W_{C2} are effective widths for circular1 and circular2 devices.

TABLE I. SUMMARY OF DEVICES IMPLEMENTED FOR OPTIMIZATION (ALL UNITS IN MICRO-METER)

$L_{g2} \backslash L_{gd}$	1.05	1.40	1.75	2.10
3.675	S, C1	S, C2	S, C2	S, C1
4.375	S, C2	S, C1	S, C1	S, C2
5.075	S, C1	S, C1	S, C2	S, C2
5.775	S, C2	S, C2	S, C1	S, C1

III. MEASUREMENT RESULTS

The high-voltage NMOS was fabricated in a commercially available 0.5µm standard 5V CMOS technology. Photomicrographs of devices are shown in Fig. 3. Two Keithley 2400 source-measure units were used for characterization. One was used to bias the transistor gate; the other one biased the drain voltage and measured drain current at the same time. Two sets of testing voltages run on the

TABLE II. TESTING CONDITIONS (ALL UNITS IN VOLTS)

Test \	$V_d(i)$	$V_g(j)$
1	0:0.1:8, 9:1:29, 29.1:0.1:50, 51:1:70	0:1:5
2	5:5:25	0:0.1:8

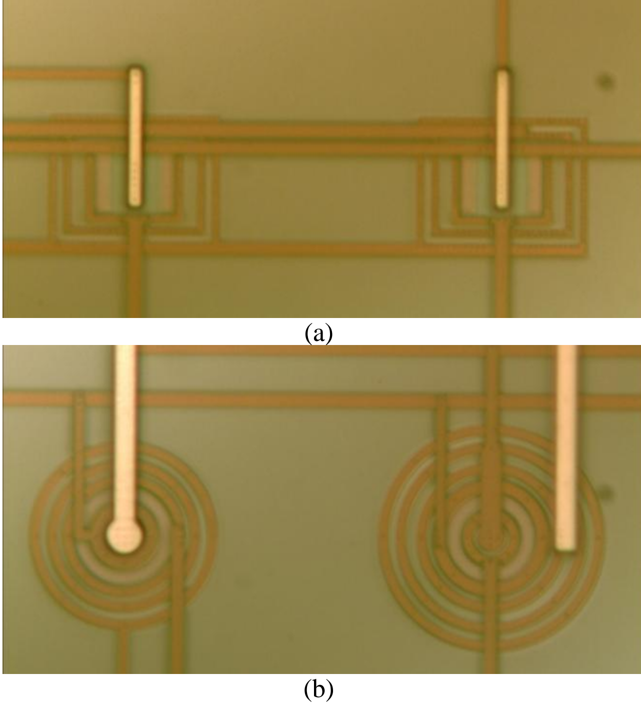

Figure 3. Photomicrographs of the devices. (a) Square structures. (b) Left: circular1 structure; Right: circular2 structure.

devices are shown in Table II, where i and j are indexes of drain voltage, V_d, and gate voltage, V_g, respectively. We use notation x:y:z to represent start voltage : incremental voltage : end voltage. In all cases body and source voltages were set to be zero.

A. Breakdown Voltage

The breakdown voltage for a single device at a specific gate to source voltage was defined as the drain to source voltage where the maximum slope occurs [8]. This was determined from measured data according to

$$V_{di}(k) = (V_d(k) + V_d(k+1))/2 \tag{3}$$

$$S_n(k) = (I_{d,n}(k+1) - I_{d,n}(k)) / (V_d(k+1) - V_d(k)) \tag{4}$$

$$V_{BD,n} = V_{di}(\arg\max_k(S_n)) \tag{5}$$

where n represents different gate to source voltages. First, the center voltages between two adjacent drain voltages were found in (3). Next, the derivative was computed as in (4). Finally, breakdown voltage was found in (5). The computations were performed on data obtained under conditions specified by Test 1. One example of such data from Test 1 is illustrated in Fig. 4. The computation results are shown in Fig. 5. Breakdown voltages were found to be highest for circular1 structures in most cases and can go above 40 V in comparison with 10.9 V for a standard transistor in the same run and <30 V for previous work using similar techniques [4].

B. Transconductance

The transconductance is defined as the derivative of drain current with respect to gate to source voltage and was

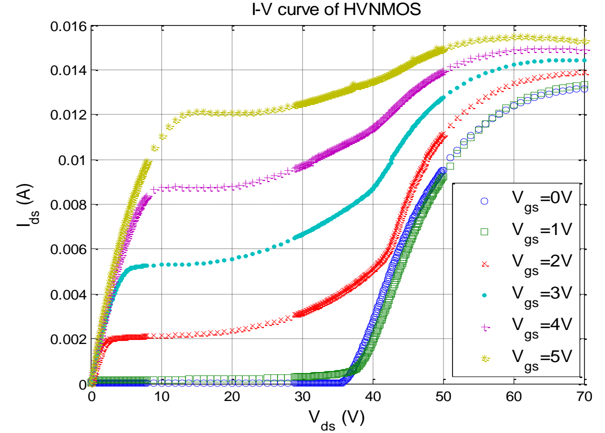

Figure 4. Measured I-V characteristic for circular1 device with L_{g2} of 3.675 μm, and L_{gd} of 1.05 μm.

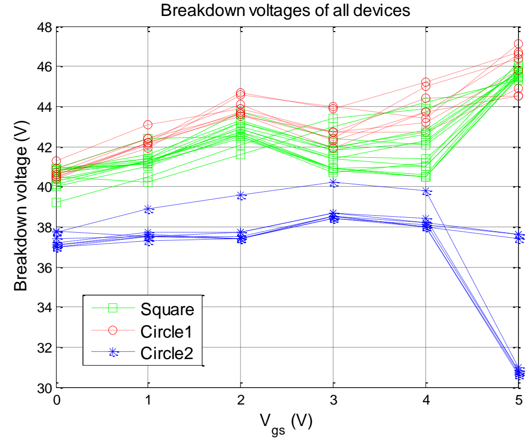

Figure 5. Breakdown voltages for circular and square structures. Circular1 structure achieves the highest breakdown voltages.

calculated data obtained under Test 2 conditions. One example of Test 2 data is shown in Fig. 6. We can see that the drain current saturates as the gate voltage goes beyond 5 V. We are still investigating this phenomenon and have not found a good explanation for it. The transconductance was normalized to a square transistor (width equals to length) and is shown in Fig. 7. The trend of the curve is consistent with the result in [6]. It reveals that the circular1 devices not only have the highest breakdown voltages but also about twice the transconductance as the square devices (141 μA/V vs. 82 μA/V at 2 V gate to source voltage). A standard square transistor in the same run has transconductance of around 40 μA/V, 160 μA/V, and 280 μA/V with applied gate to source voltages of 1 V, 2 V, and 3 V respectively.

C. Other Characterization

Measurement data from devices with L_{g2} of 3.675 μm, and L_{gd} of 1.05 μm were selected carefully to make sure the transistor is in saturation regime by assuming that the threshold voltage is less than 1.5 V. These selected data were then used for regression of the saturation current equation

$$I_d = \frac{K_n}{2}\frac{W}{L}(V_{gs} - V_t)^E(1 + \frac{V_{DS} - V_{gs} + V_t}{V_A}) \tag{6}$$

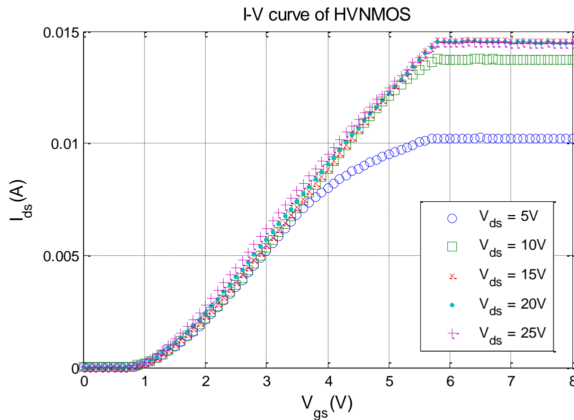

Figure 6. Measured I-V characteristic for circular1 device with L_{g2} of 3.675 µm, and L_{gd} of 1.05 µm.

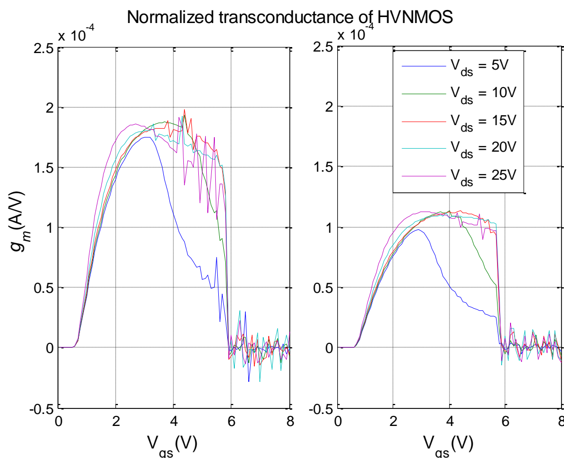

Figure 7. Normalized transconductance. Left: circular1; right: square. Both devices are with L_{g2} of 3.675 µm, and L_{gd} of 1.05 µm.

We assumed the current doesn't follow the square-law equation and used exponent E instead. The regression for the circular1 device resulted in K_n of 251 µA/V^2, V_t of 1.147 V, V_A of 132.47 V, and E of 1.104; the regression for the square device resulted in K_n of 127 µA/V^2, V_t of 1.097 V, V_A of 100.38 V, and E of 1.230. However, when the Early voltage was calculated directly from the flat region shown as the middle section of the curves in Fig. 4, the result was more than 300 V. On the other hand, when the threshold voltage was calculated directly from the data from Fig. 6, it was in the range of 0.6 V to 0.7 V. This result is more consistent with the expected value. The high-voltage devices should have the same threshold voltage level as standard transistors because their channel regions remain similar.

IV. Conclusion

This paper reports implementation results for a family of high-voltage NMOS devices. Two techniques were utilized to suppress the avalanche and surface breakdown in the transistor. Majority and minority carrier guard rings were introduced to minimize parasitic effects and isolate the devices. A total of thirty two devices in three configurations were fabricated in a 0.5µm standard 5V CMOS technology with a variety of geometries. Measurement results showed that a circular structure with a central drain has the highest breakdown voltage as well as the highest transconductance which is comparable to standard transistors in the same run. Other characterizations of the devices including threshold voltage and Early voltage were also discussed.

Our future work will focus on more extensive testing of these devices, including body effect. We also intend to develop spice models and simulation models for the device in the near future. We plan to use these models as design tools as well as research tools to further investigate the unexpected phenomena in the results such as the current saturation observed in Fig. 6.

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