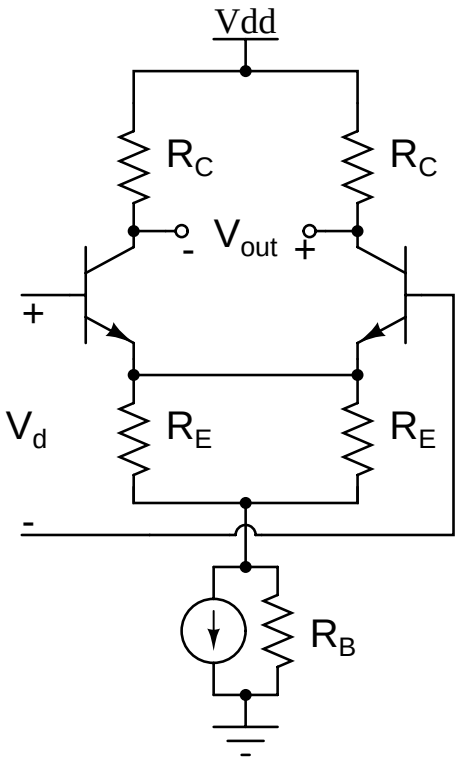
http://www.ece.umd.edu/~pabshire/enee312h.htm due Thursday, April 18, 2002

1) Circuit parameters for the following circuit are as follows: I = 2mA, V_T = 25mV, R_C = 2kΩ, R_E = 1kΩ, R_B = 10^6Ω, V_{dd} = 6V, r_μ = 0, C_μ = 2pF, C_π = 3pF, β = 100.



   a. Draw the small signal differential half-circuit models for (i) differential mode input and (ii) common mode input.
   b. Calculate the differential mode voltage gain.
   c. Calculate the common mode voltage gain.

2) Calculate the common mode and differential voltages for each of the following signal pairs:
   a. V_{IN1} = 6 V, V_{IN2} = 3 V
   b. V_{IN1} = 5 sinωt V, V_{IN2} = 0
   c. V_{IN1} = (r sinωt + 3 sinω_2t) V, V_{IN2} = 3 sinω_2t V
   d. V_{IN1} = 5 cos(ωt + θ) V, V_{IN2} = 5 cosωt V

3) – 6) Complete Sedra & Smith problems 6.40, 6.54, 6.63, 6.71

Research Question:
Most circuits designed at educational institutions in the US are fabricated through the MOSIS prototyping service. What kinds of processes are available through MOSIS? What is the range of feature sizes available? (The feature size is the smallest gate length for a MOS transistor.) When is the deadline for submitting designs for the next fabrication run, and what technology is that run? Are there any specialized processes for incorporating bipolar transistors? Compare the cost of these specialized processes, if any, with other standard processes.

Extra credit homework problem: What is I_Z (in terms of I_X and I_Y)?